

# Plasma-etching processes for ULSI semiconductor circuits

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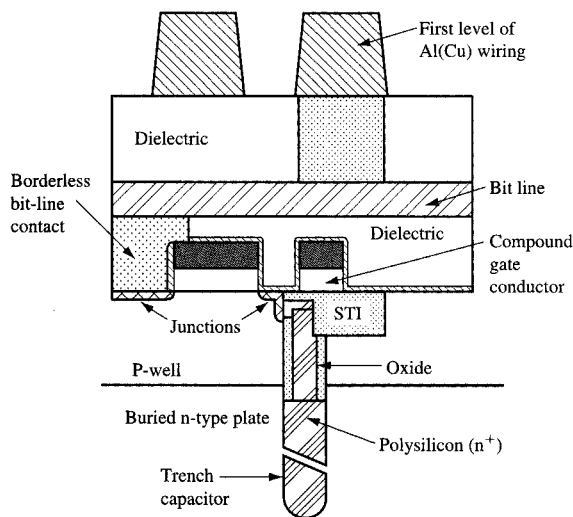
**An overview is presented of plasma-etching processes used in the fabrication of ULSI (ultralarge-scale integrated) semiconductor circuits, with emphasis on work in our facilities. Such circuits contain structures having minimum pattern widths of 0.25  $\mu\text{m}$  and less. Challenges in plasma etching in evolving to such dimensions have come from the implementation of antireflective coatings and thinner, more etch-sensitive photoresists; the increased aspect ratios needed to meet design requirements; the additional hard-mask etching steps needed at levels at which lithography is unsuitable for patterning; and increased selectivity requirements, such as the requirement that contact structures be self-aligning. Future circuit density and performance requirements dictate tighter specifications for linewidth variations permitted across a wafer, microloading effects, and device damage. As a result, plasma-etching systems for critical levels are migrating from traditional multifilm, capacitively coupled low-density-plasma systems to medium- and high-density-plasma systems employing exotic or highly polymerizing chemical species specifically designed for one type of film.**

## Introduction

Since its introduction in the 1970s [1], plasma etching has become an integral part of semiconductor integrated-circuit (IC) processing. It has become the method of choice for a variety of applications, including fine-line pattern definition, selective processing over topography, planarization, and resist stripping. The complexity of these operations has scaled directly with the dimensions of the products being processed, going from the  $>1\text{-}\mu\text{m}$  minimum pattern widths of the early 1980s to the 0.25- $\mu\text{m}$  (and lower) level of ULSI circuits. Pilot-line products are currently being developed at sub-0.20- $\mu\text{m}$  ground rules. Similarly, plasma etching has grown from the use of relatively simple, parallel-plate configurations for a variety of films, to million-dollar modular chambers with multiple-frequency generators, electrostatic chucks, externally controlled wall temperatures, and a variety of process-control sensors designed specifically for one type of film.

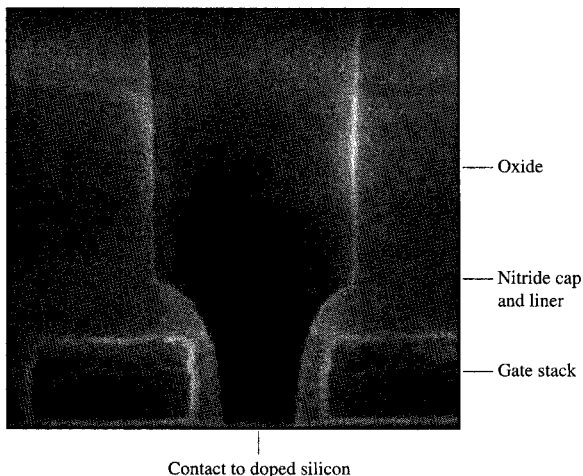
Interactions with resist/film composition, lithographic focus/exposure dose, topography, cleaning technology, and dopant profiles all play key roles in determining appropriate plasma-etching processes. As complexity has increased, these interactions have become more important and more subtle. Meanwhile, the use of more complex chemical systems has evolved as the need for selective, high-aspect-ratio anisotropic features has developed. Simple chlorine- and fluorine-based systems have evolved

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**Figure 1**

Schematic of a typical 0.25- $\mu\text{m}$ -wide trench capacitor of a DRAM cell.



**Figure 2**

SEM cross-section micrograph of a self-aligned contact (SAC) structure.

into multiple-specialty-gas selections independently controlling polymer deposition and etching. To meet these needs, etching (or simply "etch") reactors have evolved that contain highly customized sources, wall materials, pumping configurations, and temperature control facilities.

This paper reviews some of these plasma ("dry") etching process/equipment interactions and solutions in the fabrication of ULSI memory (DRAM) and logic chips. A brief overview of process and equipment issues is presented. Aspects of the following are discussed: plasma etching of silicon trenches, recesses, polysilicon gates, and Al(Cu)-based advanced plasma-etching methods. The emphasis is on work in our facility.

## Applications

Plasma etching has been used in the fabrication of semiconductor devices ranging from microprocessors to large flat-panel displays [2]. Typically, however, the process is driven by ultrahigh-density structures such as DRAM memory, which requires a low cost per bit.

Dynamic random access memory (DRAM) devices require the use of a wide variety of etching processes. Memory cells are characterized by having a transfer electrode that allows the transmission of charge through a channel to a capacitor which stores and returns charge to external circuitry. This capacitor is typically one of two types: a stacked capacitor, which rests above the transfer gate and contact levels, or a trench capacitor, for which the storage node is etched directly into the substrate [3]. **Figure 1** depicts a typical 0.25- $\mu\text{m}$ -wide trench capacitor of a DRAM cell.

Logic circuit devices do not require a large capacitor. Instead, they typically place more emphasis on critical dimensions of their gate electrode in order to increase their operating frequency. Because of the complex wiring required on logic-circuit chips, additional levels of metallization are used, placing increased emphasis on "back-end-of-line" (BEOL) oxide and/or metal etching.

All of these applications require the transfer of lithographic features to the substrate with minimal critical dimension (CD) loss, or bias. This feature is an important component of device performance, since at certain levels (e.g., at the gate electrode level) CD variations can contribute greatly to the operating frequency. Etch selectivity to different films is also essential, since resist material is occasionally inadequate to provide a sufficient mask for features which must be etched. To etch a Si trench, for example, an oxide layer must be defined as a mask for the Si, since the presence of organics during trench etching can degrade process performance. In addition to these requirements, there are other levels where very high selectivity to the underlayer is required, for example, to avoid shorting from one conducting metallization level to another. These selectivities are especially important in ULSI circuits, because in such circuits functional levels are overlapped, thus saving valuable space. **Figure 2** shows one such structure [4].

The etching processes are generally segmented by material type and function. Most common material

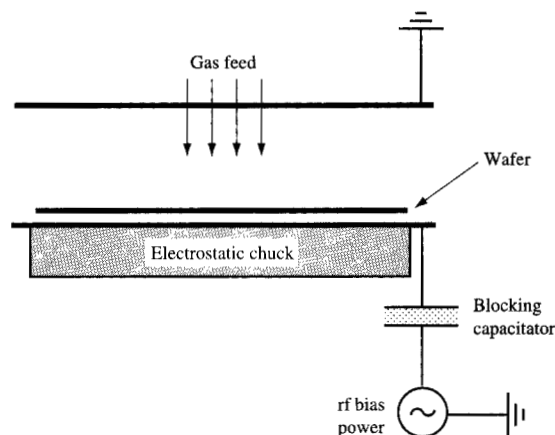
classifications include oxide, polysilicon, metal, and certain specialized resist applications. Different functions include a direct lithographic transfer into the underlying substrate, as well as isotropic planarization applications. In recent years, increasing interest in isotropic etching by chemical downstream etching has emerged as an alternative to wet etching [5]. To create the trench capacitor structure depicted in Figure 1, more than 20 different etching steps are required, utilizing a variety of distinct reactors. These delineations are required to maintain process control for critical levels, such as those for the gate electrode. They also are driven by the different chemical systems required to etch the various materials used.

Because of the fast pace of increasing chip density and the huge cost of developing higher-resolution lithography tools and resists, 248-nm lithographic tools are now being used to expose sub-0.25- $\mu\text{m}$  features, even though the wavelength of the exposure is greater than that of the printed linewidth. Since image quality is a function of both focus and exposure dose, such resolutions are obtained, in part, by minimizing the resist thickness and limiting the interference from underlying features [6]. The trend toward thinner resists is illustrated in Table 1. This reduction in resist thickness places limitations on the amount of material which can be removed during the etching. Also, since new resist formulations are required to improve the sensitivity to exposure dose, quite often resist selectivity is reduced. The most sensitive deep-UV resists etch, in some cases, 20% faster than conventional resists.<sup>1</sup>

Most of the films requiring patterning can create interference effects that narrow the lithographic process window. One of the most popular means of minimizing these effects is by using organic or dielectric antireflective coatings, or ARCs. The use of ARCs has found increasing importance as device geometries shrink. In the move from 0.35- $\mu\text{m}$ -dimension to 0.25- $\mu\text{m}$ -dimension ground rules, the number of levels requiring ARC has increased by 60%. Typically, for a given exposure tool, the ARC thickness is fixed by the lithographic process. Because the chemical systems used to etch the ARC layer also etch resist, erosion of the resist occurs during the opening of the ARC layer. Additionally, as device dimensions are reduced, design requirements dictate that the required etch depth must remain unchanged or increase. This combination of reduced resist thickness, reduced etch resistance, and static or increasing feature depth requires continuing modification of the etching process.

#### • Equipment

In recent years, etch processes have increasingly been carried out in different reactors. This has occurred primarily because of the vastly different requirements



**Figure 3**

Schematic of a traditional parallel-plate (diode-type) plasma reactor.

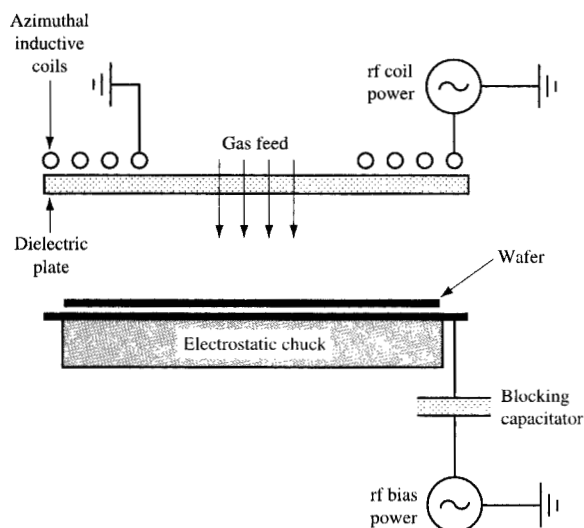
**Table 1** Photoresist and antireflective coatings (ARCs) for various DRAM generations.

| Device generation<br>(minimum gate-conductor width)<br>( $\mu\text{m}$ ) | Antireflection coating (ARC) | Photoresist thickness (nm) |
|--------------------------------------------------------------------------|------------------------------|----------------------------|
| 0.35                                                                     | No                           | 850                        |
| 0.25                                                                     | Yes                          | 600                        |
| 0.18                                                                     | Yes                          | 600                        |
| 0.15                                                                     | Yes                          | 500                        |

placed on a reactor by the particular type of material to be etched. Oxide etching requires high, energetic uniform ion bombardment with external wall temperature control. Polysilicon etching requires lower ion energies, but precise wafer temperature control. Metal etching requires the use of equipment that is resistant to corrosion. In all cases, etching systems range from traditional low-cost, diode-type reactors to more sophisticated and costly high-density-plasma systems.

Traditional diode or parallel-plate plasma reactors are well established in the industry. Figure 3 contains a schematic of a traditional parallel-plate (diode-type) reactor. Opposed plates drive the plasma in this configuration, typically at radio frequencies with an rf power in the range of kW. For the driving frequency chosen, the electrons in the reactor are preferentially accelerated, whereas the ions are driven by the average electrostatic fields. The processed wafer resides on the

<sup>1</sup> P. Hoh, R. Wise, S. Srinivasan, and Wendy Yan, unpublished results.



**Figure 4**

Typical inductively coupled plasma (ICP) reactor.

powered electrode (to enhance ion acceleration). The electron mean free path limits the operating pressure. If the pressure is lowered near the level at which the electron mean free path approaches the gap between the electrodes (generally several cm), the plasma is no longer self-sustaining. The sheaths are collisional in this case, and the ion energy and flux are coupled [7].

To provide additional flexibility, several modifications of the traditional diode reactor have been developed. For example, a triode system powers both the upper and lower electrode, typically at different frequencies. If the upper electrode is powered at a frequency much greater than the plasma ion frequency, the ion flux (plasma density) is predominately determined by the power of the upper electrode. In turn, the power of the lower electrode determines the ion energy. Alternatively, magnetic fields (magnetically enhanced reactive ion etching, or MERIE) can be applied to reduce electron diffusion toward the reactor wall surfaces, increasing the allowable mean free path of electrons available to sustain the plasma. Since the Lorentz force scales with charged-particle velocity, the highest-energy electrons are contained most tightly. Heavier species, such as positive ions, have enough momentum to overcome the curvature of the fields in most applications. These fields must be optimized to prevent excessive charge damage, and can either be electromagnetic in design or involve the use of mechanically rotating static dipole magnets.

High-density-plasma (HDP) reactors are designed so that the plasma electrons are excited in a direction parallel to the reactor boundaries. In an inductively coupled plasma (ICP) reactor, the plasma is driven by a magnetic potential set up by a coil wound outside dielectric walls (see **Figure 4**). The direction of the electron current is opposite to that of the coil currents, which are by design parallel to the reactor surfaces. Electron cyclotron resonance (ECR) and helicon sources can also be used to couple electromagnetic fields into the plasma. When the plasma is excited in this manner, the electron mean free path can become much greater than reactor dimensions, and the operating pressure can subsequently be lowered. The lower limit of the pressure is typically dictated by the particular source efficiency. In most materials processing plasmas, the electron heating is primarily resistive, and the impedance of the plasma scales with the density of neutrals available for inelastic collisions [2]. As the impedance (pressure) is lowered, so is the ability of the source to drive the plasma.

High-density sources allow the wafer platen to be powered independently of the source, providing significant decoupling between the ion energy (wafer bias) and the ion flux (plasma density primarily driven by source power). In a plasma-etching environment, the anisotropy is provided by the acceleration of ions through the plasma sheaths in a direction normal to the wafer surface. The anisotropic component is maximized when the incoming ion flux is as normal as possible to the surface. The isotropic component of the incoming ion flux is either thermal (typically less than 0.1 eV, compared to several hundred eV for the sheath voltage), or caused by collisions of the ions in the sheaths with neutrals (either elastic or charge-exchange). Operation in a lower-pressure/higher-density regime provides much thinner and less collisional sheaths, making it possible to obtain a more anisotropic etching component [2].

High-density-plasma sources may vary depending on the material to be etched. In metal and polysilicon applications, the etching is more chemical in nature, ion energies are low, and great emphasis must be placed on neutral and radical flow uniformities. In contrast, in oxide etching, the use of high-density sources which can produce more than  $4 \text{ W/cm}^2$  across a wafer necessitate the use of customized electrostatic chucks that maintain a uniform temperature across the wafer.

The primary processing advantages of high-density sources are better CD control, higher etching rates, selectivity, and an improved processing window. In general, however, the particular tool for any application is chosen on the basis of process performance and cost considerations. Because of their complexity and higher cost, these systems may not be used for less critical applications (e.g., spacer etching, planarization etching).

- *Aspect-ratio charging*

A major factor in electron-ion plasma etching of small-dimension-ground-rule, high-aspect-ratio features is the charging of dielectric surfaces (e.g., photoresist, dielectric hard-mask materials). In both diode reactive ion etching (RIE) systems and high-density-plasma systems, good uniformity and low rf biases appeared to be sufficient for achieving nearly damage-free etching. However, experience with HDP systems has indicated that uniformity and low bias are not sufficient for achieving low substrate damage and vertical etch profiles [8–12]. A number of etching problems have been encountered: polysilicon notching during over-etching of a gate electrode [8]; threshold shifts due to the etching of a polysilicon gate electrode [9]; and loss of ion current at the bottom of a via or trench etched through an insulator [10].

All of these problems are due to aspect ratio charging or electron shadowing. In almost all plasma-etching systems used today, the electrons are preferentially excited depending on the choice of driving frequency. The plasma is positively charged relative to the walls and wafer, and positive species (ions) are accelerated from the plasma in a direction normal to these surfaces. In contrast, electrons diffuse out of the plasma when the individual electron energy exceeds the plasma potential relative to the surface. In particular, when a biased surface potential approaches the plasma potential, a flood of thermal (10000–50000 K) electrons diffuses isotropically to the wafer surface. The majority of these electrons are absorbed at the upper surface of the IC features present on the wafer. Negative ions, at a much lower temperature and diffusivity, are generally unable to escape the plasma, being lost instead to recombination and detachment collisions. Thus, the ions travel to all of the horizontal surfaces, including those which are at the bottom of vias and trenches. If any portion of the etched structure and mask material is insulating, a voltage difference therefore builds up between the top surfaces of the mask and the bottom of the structures being etched. This voltage builds up until the electron and ion currents to the bottom of the structure are equal. Thus, the low-energy ions are retarded, reflected, or reflected into the walls, while the electrons are pulled down into the structure. This causes features to charge top to bottom.

As a result, ions are deflected to the sidewalls, causing notching [8]. Also, the reduced ion current [10] and energy of the ions that reach the bottom surfaces contribute an aspect-ratio-dependent phenomenon known as “RIE lag” [13], in which large features etch at a faster rate than small ones. The voltage buildup causes threshold shifts [9], and the current flow through thin insulating layers can cause oxide and device damage. These effects have been shown to worsen as the aspect ratios of the IC

structures increase [14, 15]. They can be lessened by reducing the electron temperature,  $T_e$  [16], or reducing the ratio of  $T_e$  to the ion energy.<sup>2</sup>

Some of these problems can be eliminated by using a hard mask for etching the gate electrodes, thus reducing the aspect ratio of the etch; this process is described in more detail later in this paper. Also, the etchant gas can be modified to make the sidewall protection thicker and/or more durable. This is achieved by adding a small amount of oxygen and increasing the etching bias. In via etching, the process parameters can be changed to help overcome RIE lag and selectivity problems caused by the reduction of ion current at the bottom of small or high-aspect-ratio structures. However, to continue migration toward higher-aspect-ratio structures as device sizes are reduced, other solutions may be required to minimize aspect-ratio-charging effects.

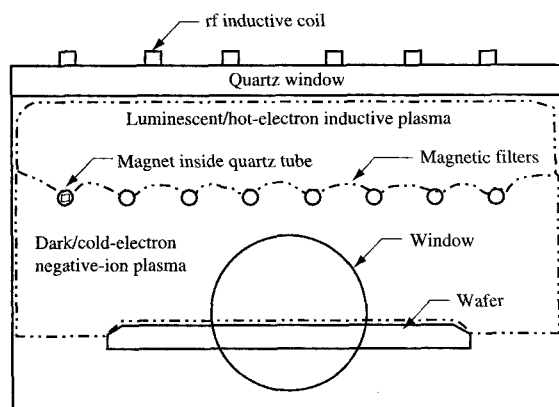
A number of researchers [9, 11] have shown that one solution is to pulse the plasma on and off with equivalent pulses  $\sim 10 \mu\text{s}$  in duration. During the off pulse, the electron temperature decreases to the order of 1 eV [18] through inelastic collisions and surface losses. Subsequently, the negative ion density increases relative to the electron density. This has been shown to reduce the notching effect [8]. If the most positive part of the rf bias is timed to occur at the end of the off pulse, the aspect-ratio-charging effects are further decreased. Samukawa and Mieno [9] have shown that the dc bias can drop to zero when the rf bias frequency is below 600 kHz. The zero dc bias and low rf bias frequency allow the negative ions to be accelerated across the sheaths. The low rf bias frequency is needed to prevent the heating of the cooled electrons and thus take advantage of the low electron temperature during the off pulse.

Keller<sup>3</sup> has suggested using a magnetic filter to reduce the temperature of the electrons in the plasma directly above the wafer. In this way, an electron temperature can be achieved that is lower than that required to sustain the plasma (of the order of 1 eV or less). Such an electron temperature would be maintained during the continuous-wave operation, not just during the off cycle. This is similar to the magnetic filters used in producing negative hydrogen ion beams for fusion devices [19]. It would also reduce radical densities. For oxide etching, Fukasawa et al. [20] have shown that lower electron temperatures near the wafer can increase selectivity, since the gas additives which “getter” the fluorine radicals in the plasma, such as HF or CFO, are not cracked to F above the wafer.

Figure 5 shows a schematic of a negative-ion-plasma RIE system. In this system the hot-electron-inductive plasma is produced by the rf coil just below a quartz

<sup>2</sup> H. H. Sawin, Massachusetts Institute of Technology, personal communication; see also [17].

<sup>3</sup> J. H. Keller, patent pending.



**Figure 5**

Schematic of negative-ion plasma RIE system.

window. The magnetic filter, which consists of a number of magnetic rods, prevents the hot electrons from diffusing into the region above the wafer while allowing the positive ions and cold electrons to diffuse. Thus, a cold-electron-negative-ion plasma is formed over the wafer. The magnetic filter may be in the form of internal or external magnetic fields. Keller, Coultas, and Zhang<sup>4</sup> have shown that the  $T_e$  of the negative-ion plasma over the wafer may be reduced by a factor of 3 or more compared to that of a conventional inductive plasma source. This means that etching would occur with a  $T_e$  of the order of 1 eV, or similar to that measured by Hahm et al. [18], for 25  $\mu$ s or more into the "off" part of a pulsed plasma. Visually such a plasma has the normal luminosity of an inductive plasma source below the dielectric window between the rf coil and the plasma. However, the negative-ion plasma over the wafer is nonluminescent because of the reduced electron temperature. To further reduce the electron temperature, the magnetic field integral of the filter can be increased or the plasma can be pulsed so that the positive part of the rf bias on the wafer occurs during the off cycle.

### Etching levels

#### • ARC etching

As mentioned earlier, lithographic patterning at sub-0.25- $\mu$ m dimensions requires very low film reflectivities in order to achieve an acceptable process window. By using ARCs, reflectivity can be minimized by absorbing the majority of the incident light or by cancellation of

interference. The ARC may be either organic or inorganic and may be implemented either above or below the photoresist (hereafter referred to primarily as *resist*). Presentation of the details of these configurations is beyond the scope of this paper; they are described in several authoritative texts and their references [21, 22]. The configuration most commonly used in the industry is the absorptive, organic, underlying antireflective coating ("bottom antireflective layer," or BARL); it is the main focus of this discussion.

An organic underlying ARC film is typically plasma-etched (or "ARC-opened") in conventional plasma-etching tools. The wafer is then etched, patterning the film. The gases utilized for ARC etching are typically oxygen-based or fluorocarbon ( $C_xF_y$ ,  $C_xH_yF_z$ )-based. The etching that occurs is predominantly chemical in nature. A heavier gas such as argon (Ar) is sometimes added to promote the sputtering component of the process. Gases such as CO, CO<sub>2</sub>, N<sub>2</sub>, and Cl<sub>2</sub> have also been used. Typically use is made of a combination of two or more gases. Other than the usual requirements for dry-etching processes (low defect density, high throughput, etc.), those for the dry etching of ARCs include

- Minimal CD bias (typically, less than a  $\pm 10\%$  change from the developed image).
- Minimal resist loss.
- Minor resist degradation during ARC etching.
- Minimal substrate loss, thereby enabling rework of the lithography if required (this requirement is application-specific and is more critical for some applications than others).

The first three points are related; the major difficulty in etching an organic ARC arises because the resist is also organic, and any chemical system used to etch the ARC will also etch the resist. While the lateral component of the etch (and thereby the CD bias change) can be controlled by tuning the dry-etching process parameters, the anisotropic etching rates of the ARC and resist tend to be similar. For DUV materials, the nature of the resist causes it to etch significantly faster than Novolac-based (MUV or I-line) materials. Hence, significant resist loss can result with common ARC open/etch chemical systems.

In Figure 6, the relative etching rates of several commercially available ARC and resist materials are shown. The data provided are for a low-power, CF<sub>4</sub>-based process using a capacitively coupled RIE chamber. Of course, this etch performance depends significantly on process parameters and may vary from one application to another. The ARC etching rates should be significantly higher than the resist etch rates. While the newer DUV ARC material tends to etch faster than the BARL, the etching behavior of the DUV resist materials tends to

<sup>4</sup> J. Keller, K. Coultas, and J. Zhang, unpublished results.

vary. Because of the low-power condition used to obtain the data in Figure 6, the biggest difference observed is an 11% higher etch rate for "Resist-5" compared to the BARL. Etch rates 35–40% higher than the BARL rate have been measured in other applications. Only one of the DUV resists has the desired lower etch rate with respect to the BARL, although the etch behaviors of some of the newer ARCs and resists are comparable.

A "D-ARC" (dielectric-ARC or CVD ARC) stands out prominently in Figure 6. It has the desired high etch rate compared to BARL and to all of the resist materials that were used to obtain the data shown. The etch behavior of the D-ARC is similar to that of any other dielectric material, and its etch performance can be tuned to provide better selectivity to the organic resist. It is important to note that the composition of the D-ARC is crucial in deriving this advantage in etch selectivity. Early results indicate that altering its composition in order to optimize its optical performance (for example, increasing the extinction coefficient to enhance light absorption) causes the etch rate of the D-ARC to change significantly.

Antireflective coating materials are still in development, and the drive toward providing improved reflectivity control is causing them to evolve at a rapid rate. From a dry-etch perspective, the primary requirements for ARC "open" processes are minimal CD change and resist and/or substrate loss. These requirements should be factored into the design of new ARC materials to ensure their successful implementation. Additionally, organic ARC etching can be considered the forerunner of more elaborate lithographic and dielectric etch options. These include top-surface imaging, use of bilayer resists, and low-*k* dielectric etching. These applications would have the same basic requirements as ARC open etching but would require more stringent control in both mask selectivity and CD control.

#### • Dielectric etching

The patterning of dielectrics, especially silicon dioxide and silicon nitride, is inherent in the manufacture of modern semiconductor devices. Because of higher bond energies, dielectric etching requires aggressive ion-enhanced, fluorine-based plasma chemical systems. Vertical profiles are achieved by sidewall passivation, typically by introducing a carbon-containing fluorine species to the plasma (e.g.,  $\text{CF}_4$ ,  $\text{CHF}_3$ ,  $\text{C}_4\text{F}_8$ ). High ion-bombardment energies are required to remove this polymer layer from the oxide, as well as to mix the reactive species into the oxide surface to form  $\text{SiF}_x$  products.

Dielectric etching applications typically rely on the competing influences of polymer deposition and reactive ion etching to achieve vertical profiles as well as etch-stopping on underlying layers [23]. As hard-mask open-feature sizes shrink to 0.18  $\mu\text{m}$ , aspect ratios are increasing to 6:1 or more. The ion and radical flux to the

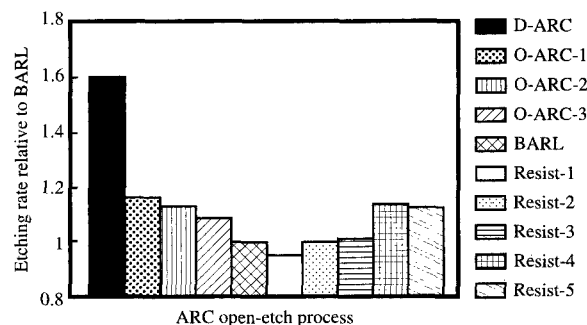


Figure 6

Relative plasma-etching rates for several commercially available DUV ARC and resist materials. The rates have been normalized with respect to the BARL etching rate; O-ARC designations pertain to organic ARCs.

bottom of these features is reduced owing to collisions with the feature sidewalls and other species present in the feature [24]. Etch products (e.g.,  $\text{Si}_2\text{F}_6\text{O}_2$  and  $\text{C}_x\text{F}_y$ ) cannot diffuse out of these features readily, resulting in excessive polymerization near the bottom of the feature, which creates highly tapered features and poor mask transfer. Another consequence of this is RIE lag [25], which, as described earlier, is seen as a variation in etch depth with feature size. Ions are lost by charging of the dielectric sidewalls [21], whereas neutral diffusion into and out of a feature is hampered by collisions with other species in the feature. Simply increasing the power to increase the ion and radical flux in a traditional system may result in unacceptable resist damage.

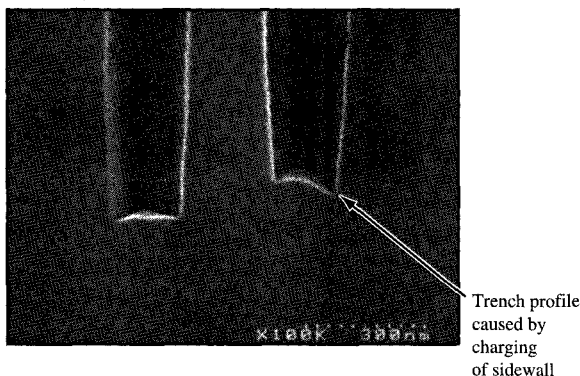
Four primary mechanisms for this loss of anisotropy and RIE lag have been identified by Buie et al. [25]:

#### 1. Ion shadowing

Scattering and charge exchange in the plasma sheath introduces isotropy to incoming ions. Decreasing the operating pressure reduces these collisions, allowing more of the incoming ion flux to reach the bottom of the feature. Also, operating in a higher-plasma-density mode, which decreases the sheath thickness [7], decreases the likelihood of an ion-neutral scattering or charge-exchange collision.

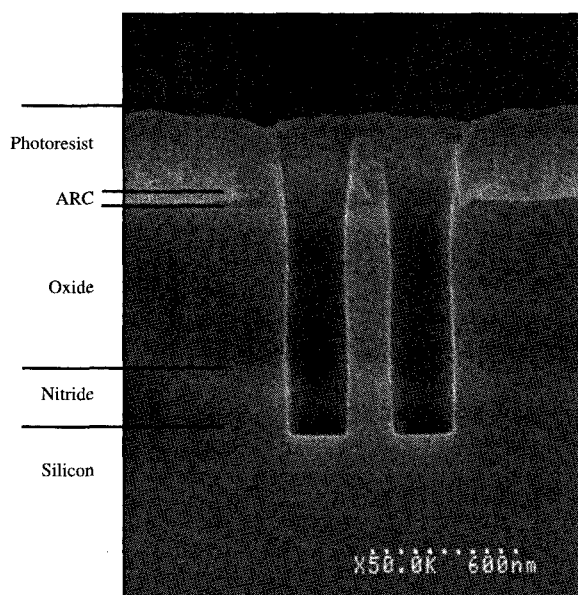
#### 2. Neutral shadowing

Collisions, either with other particles or with the feature sidewalls, inhibit the flux of reactive neutrals (e.g., F) into the feature. The flux of neutrals to the bottom of the feature, to remove deposited polymer and form volatile etch products, is hampered. Decreasing the pressure reduces this effect.



**Figure 7**

SEM cross-section micrograph showing trenching (or dovetailing) of the lower portion of a feature because of deflection of ions by charged sidewalls.



**Figure 8**

SEM cross-section micrograph illustrating nonselective dielectric plasma etching to open a hard mask for etching trenches of a trench capacitor.

### 3. Charge buildup

Electrons, because of their high diffusivity and longer mean free path, tend to preferentially charge the upper portions of etched features and resist regions. As a

result, ions are bent toward the sidewalls, which can result in trenching. This is illustrated in the scanning electron microscope (SEM) cross-section micrograph in **Figure 7**. Changes in the plasma chemical systems or ion flux can be used to alter the trenching.

### 4. Neutral product transport

The flux of etch by-products out of a feature can collide with incoming species or redeposit on the bottom of the feature, effectively increasing the polymer loading. Decreasing the operating pressure reduces this by increasing the diffusivity and volatility of the etch by-products.

Anisotropic dielectric etching is carried out in two ways: In the first, a dielectric is used as a masking layer for patterning underlying materials (see **Figure 8**). The key requirement is that the lithographic masked pattern be transferred into the dielectric with no CD change. Selectivity to the underlayer is not required and can be undesirable, since the dielectric acts as a mask during subsequent processing steps. Here, the integrity of the transferred image is paramount.

In the second, a dielectric material must be patterned *without* transferring the pattern to an underlying layer. For example, a via in silicon dioxide must often be opened down to a silicon nitride surface, which acts as an etch-stop layer to isolate underlying conductors. Here, selectivity is paramount, and the etch process (chemical systems and reactor type) is chosen to provide sufficient polymerization to protect the underlayers.

This second, selective embodiment may be further subdivided into two classes based on the topography of the underlayer. The first is a typical via/contact etch which, for example, may terminate at a flat nitride stop layer. This stop layer may be used to allow long over-etching to correct for nonuniform thicknesses of the etched dielectric film, and/or to protect underlying films which could be damaged by exposure to the etching chemical system used. For example, in **Figure 9** the patterning of a silicon nitride spacer has been performed selectively above a thin oxide underlayer. If this thin oxide is heavily eroded during the nitride etch, the doped regions may be damaged either by the etch process or by sputtering during subsequent implant steps.

The other class of selective dielectric etching is over a feature with topography, e.g., a self-aligned contact (SAC) etch over gate structures. As seen in **Figure 2**, in this "borderless" etch the underlying nitride cap and liner are used to protect the gate conductor from shorting to the contact conductor. Here selectivity is required at the bottom of the feature, on the sidewalls, the corners, and the upper portions of the gates. Achieving selectivity here is much more demanding because the protective polymer films and the underlying substrate molecules tend to



sputter more easily off angled corner surfaces than flat surfaces [13, 26, 27].

#### High-aspect-ratio dielectric etching

There are an increasing number of high-aspect-ratio dielectric applications in IC fabrication, especially with the recent interest in damascene processing. A number involve etching dielectrics, especially oxide, with high aspect ratio and vertical profiles. One of the most challenging of these types involves imaging the hard mask used for the trench capacitor etch (see Figure 8). In this application, resist is applied on a  $\text{SiO}_2/\text{Si}_3\text{N}_4$  stack, which is used as a hard mask for etching deep silicon trenches. The thickness of the  $\text{SiO}_2$  is fixed by its erosion rate during the trench etching. Typically, this thickness is  $\sim 0.5 \mu\text{m}$ . The nitride thickness is  $\sim 0.2 \mu\text{m}$ , and is determined by other integration concerns. Since the ground rules for this level are at minimum lithographic dimension, aspect ratios can be high ( $>6:1$ ).

A major issue confronting this level is the implementation of deep ultraviolet (DUV) lithography to sub- $0.20\text{-}\mu\text{m}$  ground rules. With larger-ground-rule processes ( $>0.25 \mu\text{m}$ ), species can be etched with a larger process window, because thicker resists are used. As the resist thickness shrinks with the ground-rule change, problems begin to appear. At smaller dimensions, optical lithographic definition of on-pitch trenches requires a thin, etch-sensitive resist. As mentioned previously, the additional etching of an organic or dielectric antireflective coating (ARC) layer consumes additional resist. In this application, an ARC layer  $\sim 0.10 \mu\text{m}$  thick has been used.

The hard-mask open-etching process consists of an ARC step followed by a two-step dielectric process. In  $0.18\text{-}\mu\text{m}$  applications, resists are thin enough ( $\sim 0.6 \mu\text{m}$ ) that facets are introduced into the resist during the etching process which can transfer into the masked image. Additionally, under certain conditions, morphological changes to the resist can cause masking of the substrate which can later cause "microfissures," leading to yield or reliability problems. Therefore, the etching process must be designed to avoid excessive consumption/damage of resist while still providing sufficient energy to form volatile silicon dioxide products. All of this must be done while maintaining tight critical dimension control.

The ARC etch typically consists of a mixture of  $\text{O}_2$  and fluorocarbon compounds. When a conventional process is used on structures with thin resist, microfissures appear. An SEM image of an oxide surface containing microfissures after exposure to an rf plasma is shown in Figure 10. The sample containing the oxide was processed with 800–1100 W using a  $\text{CHF}_3/\text{CF}_4$  system in a capacitively coupled MERIE reactor. The resist used was a positive resist with a post-develop baking temperature of  $95^\circ\text{C}$ .

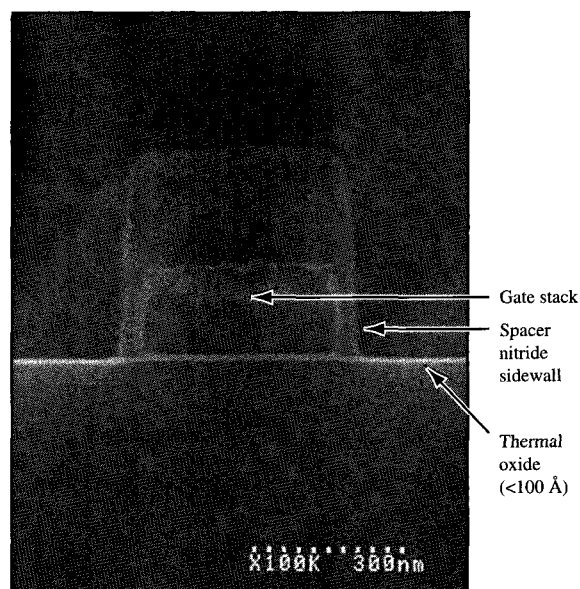


Figure 9

SEM cross-section micrograph illustrating selective nitride plasma etching to pattern a silicon nitride spacer.

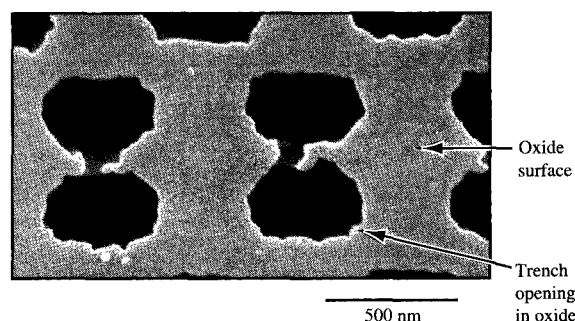
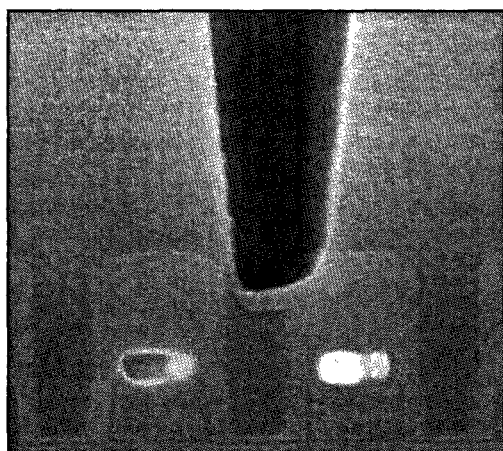


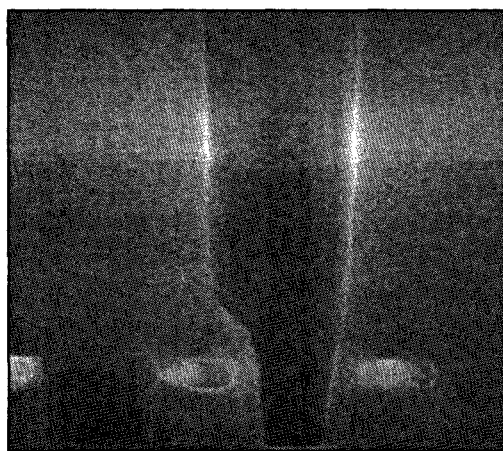
Figure 10

SEM of an oxide surface after aggressive etching for creating openings (dark regions) for trench etching.

At this time, the exact origin of these microfissures is uncertain. One possibility is that they are caused by interactions between the deep-UV resists and background plasma radiation, thus forming a skin layer that acts as a micromask [28]. Their appearance also depends on the amount of reactive species in the plasma, which can



(a)



(b)

**Figure 11**

SEM cross-section micrographs illustrating (a) etch stop in oxide etching resulting from excessive polymer during  $C_4F_8$ -based etching of a self-aligned contact structure; (b) elimination of the etch stop with the addition of  $O_2$ .

accentuate micromasking, as well as the bias power of the reactor, which can sputter resist corners, thereby leaving a jagged profile.

Although the primary mechanism for improving resist integrity is not currently known, process optimization can result in an improvement, but also a reduced etching rate. For some MERIE reactors, this can be offset by increasing magnetic field strength, which increases ion density [7]. However, magnetic field strength is limited by wafer uniformity, which is determined by the reactor design and the chemical system used.

Etching processes designed to maintain resist integrity, as described above, can exhibit a large degree of image

taper. In the case in which excessive polymerization occurs near the bottom of a structure, the CD loss can be as much as  $0.04 \mu m$ . This loss is predominantly caused by taper in the nitride layer, both because the nitride etch has the highest aspect ratio and the polymer deposition on the nitride is thicker than on the oxide [29]. Increasing the ion flux or decreasing the polymerization improves the anisotropy, but can cause increased resist damage and microfissures (Figure 10).

Further improvement in resist selectivity can be achieved by using more selective chemical systems (e.g.,  $C_4F_8$ -based systems). These systems, frequently used in contact applications, can lead to a higher risk of etch stop because of additional polymer deposition, as shown in **Figure 11(a)**. A polymer scavenger gas such as  $O_2$  can be introduced to control the amount of polymer deposition on the wafer. **Figure 11(b)** shows a feature etched with such a gas mixture. However, if too much  $O_2$  is added, this approach can result in excessive resist erosion. Similarly, increasing the power or decreasing the pressure can increase the flux to the substrate, avoiding the occurrence of etch stop. This adjustment, however, can in turn increase the amount of resist damage.

The opposing trends of etch stop versus microfissure formation are difficult to control using a capacitively coupled source. This is because the ion flux, energy, and plasma chemistry are coupled, making it difficult to achieve high rate, low resist damage, and good CD control/uniformity simultaneously. Inductively coupled reactors provide more flexibility in difficult applications such as hard-mask etching.

Semiconductor equipment manufacturers have developed high-density systems to address many of the issues related to anisotropy. In a high-density system, the operating pressure can be much lower (5 mTorr or less), and the diffusivity and mobility of the reactive species correspondingly higher. RIE lag due to ion and neutral shadowing, as well as neutral product transport, is reduced. In addition, the ion flux is independently tunable by the source power, so that the total ion flux can be increased without as much of an increase in the ion energy, potentially reducing resist damage.

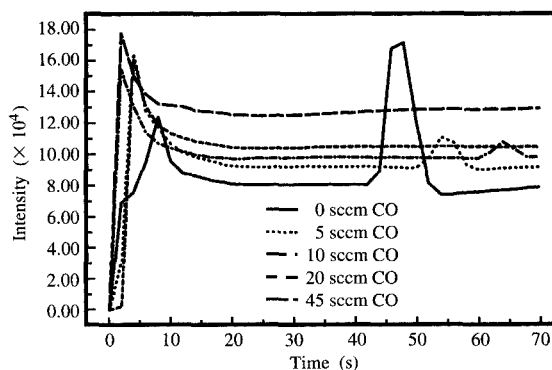
In developing a process for an inductively coupled reactor (ICP), we have retained the optimized capacitively coupled ARC open step ( $CF_4$ -based system) mentioned earlier. However, it was necessary to incorporate an additional "de-scum" step following ARC open when an ICP was used for oxide etching. In a capacitively coupled reactor, the sheath potentials are generally much larger [2] and more easily sputter off any residual polymers from the ARC open process. As a result, a low-power (<300-W bias)  $He/O_2$  (70%/30%) de-scum step was developed and has been used prior to bulk etching in an ICP system (with only minimal impact on microfissure formation).

Employing traditional chemical systems (e.g.,  $\text{CF}_4/\text{CHF}_3$ ) in a high-density-plasma (HDP) chamber may lead to excessive resist loss/damage. This occurs because the higher ion flux removes too much of the polymer protecting the resist. The greater dissociation efficiency and high ion flux of high-density-plasma sources permits the use of a more highly polymerizing feed gas (e.g.,  $\text{C}_4\text{F}_8$ ). While etch stop is still a concern, the ability to tune the ion flux and energy results in more process latitude. Because of their low operating pressures (i.e., increased species diffusivities), chamber wall conditions play a more important role in HDP reactors [30, 31]. For example, to control polymer buildup on the walls, the wall temperature is regulated, and  $\text{O}_2$ -based cleaning steps are used prior to processing a wafer. It has been shown that during a typical HDP etching process as much as 3000 Å/min of polymer is deposited on unbiased surfaces, leading to a transient state of the system during etching [32].

A well-established HDP silicon dioxide etching system contains a noble gas (Ar or He),  $\text{C}_4\text{F}_8$ , and  $\text{C}_2\text{F}_6$ . Several possible mechanisms for the Ar/ $\text{C}_4\text{F}_8$ / $\text{C}_2\text{F}_6$  etching of oxide have been proposed [13, 33]. Since  $\text{C}_4\text{F}_8$  is a strained ring molecule, dissociation products are expected to consist of high levels of  $\text{CF}_x$  ( $x \leq 2$ ) polymer precursors. On the other hand,  $\text{C}_2\text{F}_6$  is a linear molecule and probably provides a higher fraction of  $\text{CF}_3$  chain terminators. In any event, the chemical mechanisms involved are dependent on the specific process used, the plasma density, and the electron temperature.

Etching a hard-mask oxide with Ar/ $\text{C}_4\text{F}_8$ / $\text{C}_2\text{F}_6$  does indeed lead to sidewall profiles (see Figure 8) that are better than those obtained by means of traditional systems ( $\text{CF}_4/\text{CHF}_3$ ) in diode-type reactors. Increasing the  $\text{C}_4\text{F}_8/\text{C}_2\text{F}_6$  ratio increases both the oxide taper and resist selectivity (increased polymer). In many cases the resist selectivity is inversely proportional to the oxide etching rate. The exact mechanisms remain unclear, but it is reasonable to expect that oxygen-containing etch products can contribute to a loss of photoresist. Dilution of the reactive gases or reduction in the bias power both decreases the oxide etching rate and increases the selectivity to resist. This combination of resist selectivity, oxide etching rate, and oxide taper angle must be optimized for each particular application.

The oxide etch can have an even greater effect on resist integrity in an HDP reactor. Because of the higher densities in an HDP reactor, significantly greater amounts of polymer can be deposited on the wafer at much higher temperatures. This combination can have devastating effects on resist integrity. For example, a highly selective  $\text{C}_4\text{F}_8$  process was used to etch an oxide film. The polymer created during the etch accumulated on the resist, helping provide resist selectivity. This accumulation of polymer effectively prevented volatile by-products from the resist



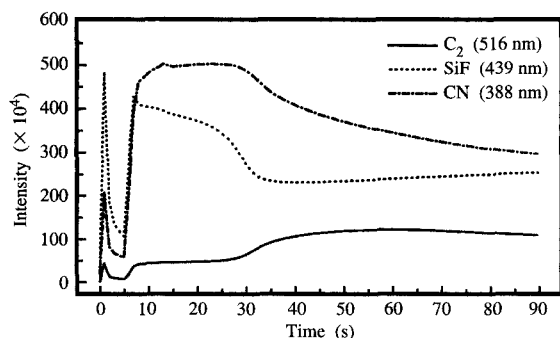
**Figure 12**

Optical emission traces for hydrogen, indicating the amount of  $\text{H}_2$  released over a period of time with various amounts of CO present in a  $\text{C}_4\text{F}_8$  high-density plasma.

and underlying substrate from escaping. After an extended period of time, heating of the wafer caused these by-products to erupt. **Figure 12** shows an optical emission signal (OES) for hydrogen over a period of time from such a reaction with the addition of different amounts of CO. The addition of CO reduces the selectivity of the etch in this case. It is believed that the reduction of  $\text{H}_2$  emission (or resist "popping") is due to a reduction in polymer formation on the surface of the resist, reducing selectivity and thus permitting volatile species to escape.

This phenomenon can be corrected by adjusting the composition of the resist to minimize volatile by-products, by adjusting the chemical system such that the polymer capping the resist does not totally seal off species from outgassing, or by increasing the wafer cooling to minimize outgassing. The latter approach may require substantial equipment changes, since better wafer back-side cooling via He flow would require larger e-chuck forces to prevent He leakage.

Etching of silicon nitride in an HDP system is less well established. A conventional approach is the addition of an  $\text{O}_2$  to the aforementioned Ar/ $\text{C}_4\text{F}_8$ / $\text{C}_2\text{F}_6$  mixture. This, however, leads to damage of sensitive DUV photoresists. Possible mechanisms are an increase in the chemical attack of the resist and a decrease in the thickness of protective polymer layers.  $\text{O}_2$ -free gas mixtures are required to provide adequate protection of the photoresist and additional chemical or reactive-ion-etching components for the nitride. The results of using such a process were shown in Figure 8. There was no measurable CD loss in the nitride, and the overall resist selectivity was improved over the low-density source. Some of the



**Figure 13**

Illustrative changes over a period of time in optical emission traces from an HDP system operating with poor thermal control.

**Table 2** Some process characteristics for deep-trench mask opening; low- and high-density-plasma reactors are compared.

| Metric                    | Low-density-plasma reactor | High-density-plasma reactor |
|---------------------------|----------------------------|-----------------------------|
| CD loss (nm)              | 40                         | ≤5                          |
| Oxide etch rate (Å/min)   | 40                         | 120                         |
| Nitride etch rate (Å/min) | 15                         | 65                          |
| Photoresist selectivity   | 2.5:1                      | 2.9:1                       |

characteristics of the process are listed in **Table 2**. Note that the throughput of the HDP source is more than three times that of the low-density source, justifying its higher initial cost.

#### Selective dielectric etching

Traditional dielectric etching gas combinations (e.g.,  $\text{CHF}_3/\text{CF}_4$ ) have been used in the past to provide selectivity during oxide etching to silicon underlayers. Aggressive structures, requiring an oxide etch stop on nitride or nitride stopping on oxide, have come to play an increasingly important role in modern device fabrication. Because of capacitance concerns, the stop layer may be quite thin, ranging from a few hundred Å to less than 50 Å in advanced logic applications. In general, selectivity can be achieved either by selective deposition of a polymer on the underlayer or by employing a chemical combination which does not volatilize the underlayer. Processes which rely on polymer deposition must be properly tuned to avoid operating near an etch-stop point,

where the rate of polymer deposition exceeds the rate of polymer removal.

**Selectivity to silicon nitride** Selectivity to nitride, and in particular selectivity to nitride over topography, is a key issue for production-worthy oxide-etching systems. For oxide etching, fluorocarbon-based chemical combinations are used to selectively deposit a protective polymer layer to achieve selectivity. Two mechanisms can be proposed whereby the polymer deposited on oxide is selectively removed. Combustion with surface oxygen can occur in a shallow ion-bombardment-induced "mixing layer," or a different sticking coefficient of the polymer on various surfaces can cause the polymer to be more easily sputtered from oxide surfaces. A chemical component may also be included, as the etching rate of silicon dioxide is generally much more weakly dependent on temperature than is the silicon nitride etching rate. The etching rate of silicon nitride is typically higher at lower wafer temperatures [13].

The most aggressive structures are self-aligned contact (SAC) etches (see Figure 2). In these applications, exposed corners, high-aspect-ratio features, and the necessity to etch between gate structures (where spacing can drop to less than 0.1  $\mu\text{m}$  on 0.18- $\mu\text{m}$ -ground-rule devices) combine to require very robust etching processes. Device topology can cause the oxide layer thickness to be uneven, leading to an artificially high over-etching requirement (as much as 50%). Interactions with sensitive DUV resists may upset the polymer balance during etching, increasing the likelihood of etch stop in small features. Similarly, the walls of the etching chamber can act as an additional source of polymer and increase the tendency to etch stop. This is especially true for HDP systems operating with poor thermal control because of high species diffusivities and repetitive deposition and volatilization of polymer precursors on walls. **Figure 13** depicts optical emission traces for  $\text{C}_2$ , SiF, and CN from an HDP operating with poor thermal control. The traces are for critical polymer, etchant, and product species, respectively. At initial wall temperatures, the cold walls act as a polymer sink, depressing selectivity. As the wall temperature increases over time, polymerizing species are both contained in the plasma and desorb from the walls, causing dramatic changes in the composition of the plasma and, subsequently, substrate selectivity.

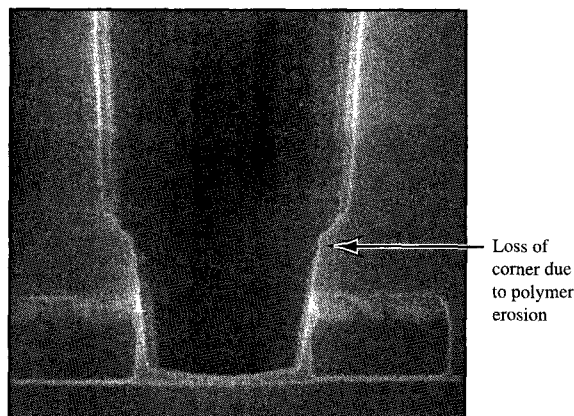
In order to achieve high selectivity, it is necessary that all reaction products be quickly removed from the reactor to avoid redeposition or chemical attack of the underlayer (e.g., oxygen-containing by-product attack of the nitride polymer layer). The pumping rate scales approximately with the flow rate and inversely with the operating pressure. In some instances this may lead to nonuniformity

in the etching process in the direction of the pumping apparatus. Baffle plates may be installed to distribute the flow fields in a radial symmetric manner, but polymerization and subsequent loss of conductance through these plates can drive frequent chemical cleaning requirements, increasing the cost of ownership of the tool. Low-pressure systems, operating with high total gas flows, may suffer more from etch nonuniformities in the direction of the pumping port if convective flow becomes important compared to diffusive flow.

Recently, highly polymerizing processes (e.g.,  $C_4F_8$ -based processes) have become more common in providing selectivity to silicon nitride [21]. In particular, MERIE systems employing mixtures of  $C_4F_8$  and CO have provided both good "blanket" (30:1) and corner selectivity. For conventional diode-driven etching systems, only MERIE reactors with a sufficiently high dc bias (i.e., anode-to-cathode ratio and bias power) and sufficiently small residence times provide adequate corner selectivity [32]. Extension of this process to sub-0.25- $\mu\text{m}$ -ground-rule features has required a reduction in the  $C_4F_8$  flow to reduce the tendency toward etch stop. At such smaller ground rules, the  $C_4F_8$  concentration must be reduced to the point where corner selectivity is compromised, as seen in **Figure 14**. Although polymerization is expected to play a role in the selectivity, another mechanism must also be important, since polymer created from interaction with the resist does not substantially alter the selectivity. The chemical etch rate of silicon nitride can also be used to improve selectivity by operating at higher wafer temperatures, thus reducing the relative etch rate of  $Si_3N_4$ . Temperature control must be used cautiously because increased volatilization from DUV photoresist may also increase the tendency toward etch stop.

Another proposed mechanism to obtain selectivity to silicon nitride requires the implantation of carbon into the nitride layer. Sekine et al. [13] have demonstrated that exposed silicon nitride implanted with C atoms from a  $C_4F_8$ /CO-based MERIE plasma displayed a reduced etch rate. Furthermore, they demonstrated through an isotopic analysis that the source of the C atoms was CO, although the exact mechanism of implantation remains unclear. The addition of CO led to a much larger  $C^+$  signal in appearance mass spectroscopy (AMS). This etching system was shown by Sekine to be extendible in principle to 0.15- $\mu\text{m}$  contacts through the addition of small amounts of  $O_2$ . The proposed role of the  $O_2$  addition is to aid in polymer removal and prevent the occurrence of etch stop. It is not clearly understood whether such addition causes an undue loss of corner selectivity, and whether this process has an adequate window at the smaller ground rules.

In contrast to the MERIE applications, the current high-density-plasma processes used at IBM (with  $Ar/C_4F_8/C_2F_6$  mixtures) rely primarily on a protective



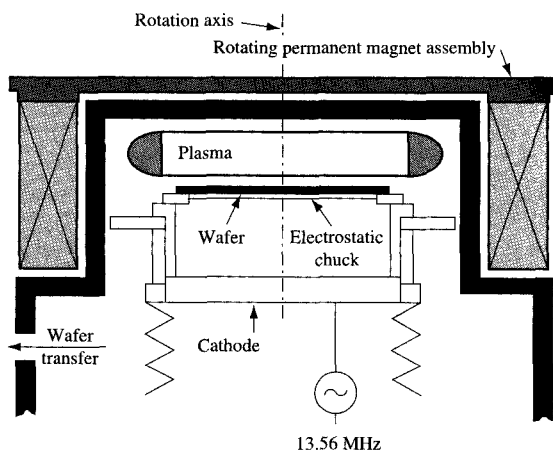
**Figure 14**

SEM cross-section micrograph of a self-aligned contact opening etched in an HDP system, illustrating poor corner selectivity resulting from reduction in  $C_4F_8$  concentration.

$C_xF_y$  polymer layer to provide selectivity.<sup>5</sup> These processes provide a thick polymer layer, as shown by measurements using electron microscopy and X-ray photoelectron spectroscopy (XPS). The role of polymerization and interaction of resist is clearly demonstrated by low blanket selectivity (5:1 or less for blanket wafers, 20:1 or higher with resist present). Achieving corner selectivity with such a process can be more difficult because of sputtering of the protective polymer from the corners (see Figure 14). The process window between etch stop and loss of corner selectivity may be too small to allow for sufficient over-etching. In addition, temperature control of the chamber is critical. Owing to the low operating pressure, species diffusivities are high, and outgassing from surfaces can have a severe effect on the etching process.

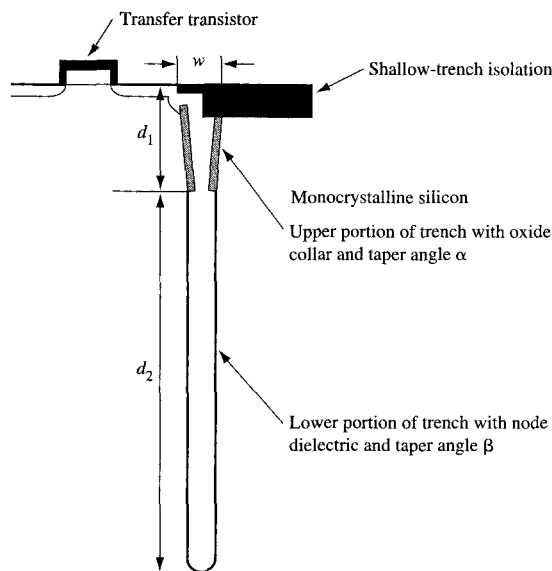
Recently, improved selectivity to nitride corners during SAC etching has been demonstrated with the addition of hydrogen to the  $C_4F_8$ -based system. It has been shown that increasing corner selectivity correlates with a shift from C-C to C=C bonds in the polymer layer, as well as an increase in C content and  $C_2$  emission in the plasma, suggesting a more carbon-rich and adherent polymer layer [34]. The polymer thickness is greater for the hydrogen-containing system in both MERIE and HDP sources than for the  $C_xF_y$  polymer formed without hydrogen. An HDP source is preferable in these highly polymerizing applications, since the tendency toward etch stop in the oxide etching process can be minimized, as previously mentioned. Finally, it should be noted that the

<sup>5</sup> M. D. Armacost, J. Diang, D. B. Dobuzinsky, R. Hung, B. Spuler, B. Tang, R. S. Wise, and J. Wittmann, unpublished results.



**Figure 15**

Schematic of parallel-plate dipole rotating magnet (DRM) reactor. From [39], with permission.



**Figure 16**

Features of DRAM Si trench capacitor used in the 256Mb DRAM chip developed by IBM, Siemens, and Toshiba. From [38], with permission.

chemical vapor deposition (PECVD), and as the use of the nitride is replaced by advanced integration schemes.

**Selectivity to silicon oxide** As device dimensions continue to shrink, novel structures have been devised to meet design rules. For example, in a "nitride spacer etching" process, a thin sidewall spacer is formed adjacent to the device gates (see Figure 9), providing a low-density doped region adjacent to the gate in subsequent ion implantation steps. In this application the nitride (typically several hundred Å thick) must be etched very selectively with regard to the underlying thermal oxide layer, which may be less than 50 Å thick. Achieving selectivity to oxide can be a much more difficult task, since the oxygen content of the silicon dioxide tends to combust surface polymers if the ion mixing level (ion energy) is too great. In nitride etching, either of the following may be used to achieve selectivity: using etching processes which do not form volatile products with silicon dioxide but do with nitride, or providing a polymer layer which either etches or sticks less efficiently on the nitride layer than on oxide.

Using the chemical approach,  $\text{Cl}_2$ -based etching processes afford good selectivity to oxide (10:1) but poor selectivity to silicon (0.2:1 or less). In the event of a punch-through of the underlying oxide, the  $\text{Cl}_2$  would rapidly attack silicon, and especially the doped silicon located beneath spacer structures. The etching rates tend to be high, and hence it is sometimes difficult to stop etching on the oxide layer reliably. Nevertheless, this approach has the advantage of being indifferent to polymer-deposition mechanisms, simplifying the process development.

Fluorocarbon-based etching processes have recently been developed [35, 36] which offer similar selectivity to oxide, very good selectivity to silicon (as much as 20:1), and more controllable etch rates than  $\text{Cl}_2$ -based processes. The exact mechanism is poorly understood, although generally hydrogen-rich fluorocarbons are required (e.g.,  $\text{CH}_3\text{F}$ ,  $\text{CH}_2\text{F}_2$ ) with some oxidant (e.g.,  $\text{CO}$ ,  $\text{CO}_2$ ). It has been proposed that such species form thick, easily sputtered films. The bond energy for silicon nitride is lower than for silicon dioxide, and these fluorocarbon processes use low ion-bombardment energies (i.e., low bias powers) to achieve selectivity. Low ion energy helps ensure that the polymer is not consumed as readily by combustion in an oxide mixing layer. Another possible model is that the hydrogen-rich films adhere better to the oxide, and the ion energy is tuned to provide an intermediate energy sufficient to remove the nitride film but too low to sputter the oxide film.

Implementation of fluorocarbon-based  $\text{Si}_3\text{N}_4:\text{SiO}_2$  selective etching requires strict control of etching-chamber surfaces, since any polymer introduced from the walls

requirements for selectivity are growing more stringent, as the nitride deposition process advances from low-pressure chemical vapor deposition (LPCVD) to plasma-enhanced

of the chamber may influence the surface chemistry. Generally, both the polymer deposition rate and the etching rate of the silicon nitride are highly sensitive to wafer temperature, and current electrostatic chuck temperature uniformity may not always be sufficient.

A multitude of other dielectric etching systems are used throughout a DRAM or logic process. However, discussion of all of these in detail is too lengthy to consider here. In general, however, application of these principles for both classes of dielectric etching processes is sufficient to meet the needs of the integrated process flow.

#### • Silicon trench etching

While dielectric etching typically drives the largest number of applications in the fabrication of an IC wafer, Si applications define features critical to device performance. The deep-trench storage node capacitor used in some DRAM structures is one of these critical features [2]. Trench etching is typically carried out as an RIE process with a  $\text{SiO}_2$  hard mask, as discussed earlier. In this work, a well-established magnetically enhanced RIE system (MERIE) and a dipole rotating magnet (DRM) reactor (shown in Figure 15) were used. The primary metrics considered in trench etching include a high etching rate even for ultrahigh-aspect-ratio features and control of trench taper angles to very tight limits.

Figure 16 shows features of the trench capacitor used in the 256Mb DRAM chip developed by IBM, Siemens, and Toshiba [3, 38]. After trench etching, the trench depth  $d$  is  $\sim 8 \mu\text{m}$ , comprising an upper portion of depth  $d_1$  and a bottom portion of depth  $d_2$ . In a top-down view, the trench is oval in shape, with a width  $w$  being  $0.34 \mu\text{m}$  and a length  $l$  being  $0.56 \mu\text{m}$ . There are two different taper-angle requirements for the upper and lower portions. The taper angle  $\alpha$  of the upper portion must be less than  $89.0^\circ$  in order to prevent seam formation in the polysilicon fill at the upper portion. To maximize the capacitor surface area, the lower taper angle  $\beta$  must be as large as possible [39]. Table 3 shows nominal values of capacitor surface

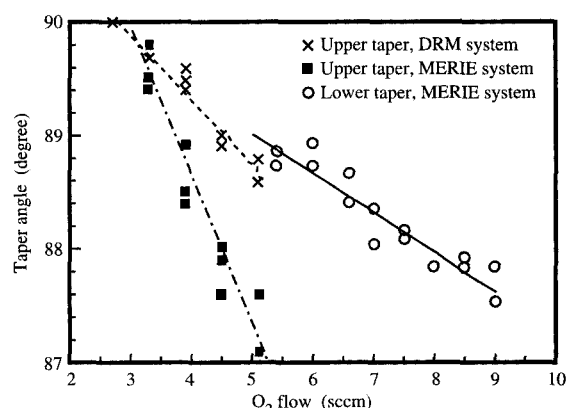


Figure 17

Taper-angle control through dependence on  $\text{O}_2$  flow, for MERIE and DRM systems. From [38], with permission.

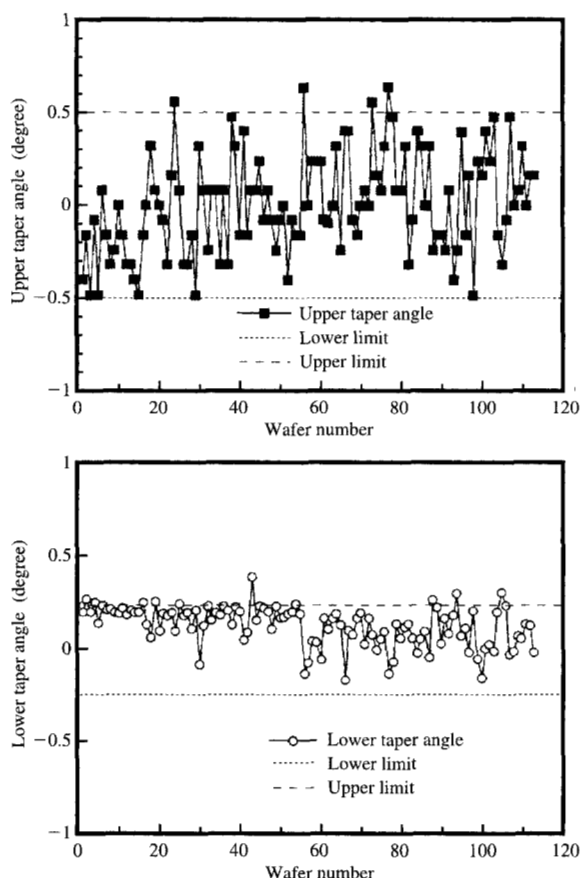
areas for different DRAM generations. The values for  $\alpha$  and  $\beta$  increase with each generation in order to avoid the pinch-off of trenches at their lower portions before reaching their required depths.

The main factors controlling the taper angles are the  $\text{O}_2$  partial pressure in a  $\text{HBr}/\text{NF}_3/\text{O}_2$  etching process and the wafer surface temperature. The  $\text{O}_2$ , together with Si-containing etching products, forms a sidewall passivation layer. The growth rate of this layer is temperature-dependent. The deposition of the layer decreases the size of the opening and thus determines the taper angles. Figure 17 shows the dependence of  $\alpha$  and  $\beta$  on the  $\text{O}_2$  flow for MERIE and DRM systems. Upper and lower taper angles can thus be altered by adjusting the  $\text{O}_2$  flow. Notice that the sensitivity of the upper taper angle to oxygen-flow variations is reduced in the case of the DRM system, mostly due to the fact that the DRM system

**Table 3** Trench shape variations for different DRAM generations resulting in a  $\pm 10\%$  capacitor surface-area change by deviations of parameters from their nominal values. Extrapolated values are indicated for 1Gb and 4Gb DRAMs. From [38].

| DRAM generation | Parameter         | Width $w$ (nm) | Depth $d_2$ of bottom part ( $\mu\text{m}$ ) | Top taper angle $\alpha$ ( $^\circ$ ) | Bottom taper angle $\beta$ ( $^\circ$ ) | Surface area of bottom part ( $\mu\text{m}^2$ ) | $C_{eq} = 5 \text{ nm}$ (fF) | $C_{eq} = 3.8 \text{ nm}$ (fF) |
|-----------------|-------------------|----------------|----------------------------------------------|---------------------------------------|-----------------------------------------|-------------------------------------------------|------------------------------|--------------------------------|
| 256 Mb          | Nominal deviation | $380 \pm 26$   | $6.2 \pm 0.75$                               | $88.4 \pm 0.5$                        | $89.65 \pm 0.24$                        | $6.84 \pm 10\%$                                 | 47                           | 62                             |
| 1 Gb            | Nominal deviation | $269 \pm 20$   | $5.94 \pm 0.72$                              | $88.65 \pm 0.54$                      | $89.75 \pm 0.19$                        | $4.89 \pm 10\%$                                 | 34                           | 45                             |
| 4 Gb            | Nominal deviation | $190 \pm 14$   | $5.85 \pm 0.71$                              | $88.8 \pm 0.55$                       | $89.8 \pm 0.14$                         | $3.44 \pm 10\%$                                 | 24                           | 31                             |





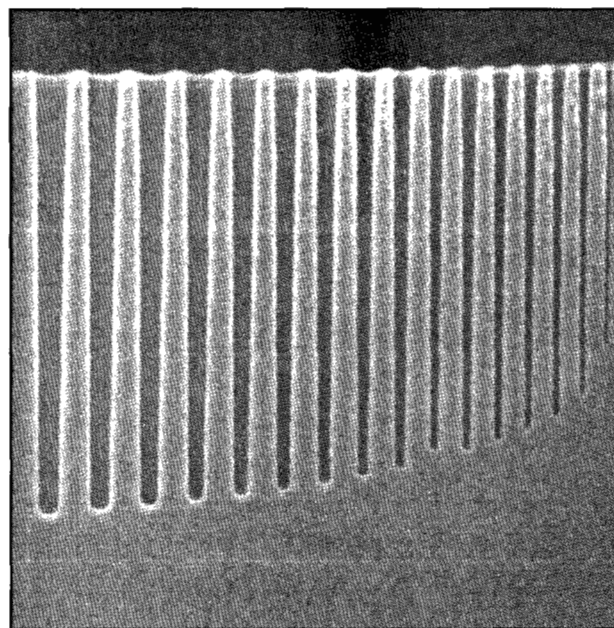
**Figure 18**

Upper and lower taper-angle variability for wafers processed in an MERIE system during a year. From [38], with permission.

utilizes a higher total gas flow than the MERIE system. A higher flow conductance of the DRM chamber allows centering the DRM process at a higher flow level.

The cathode coolant temperature adjusts the wafer surface temperature. A 10°C coolant temperature results in a reduction of ~0.15° in the upper taper angle. However, due to the slow response time of coolant temperature change, it is preferable to control the surface temperature of a wafer by altering the He back-side pressure. A change of the back-side pressure alters the heat transfer from the wafer to its cooled chuck [40]. **Figure 18** shows taper-angle data obtained from 120 wafers during a one-year period. The 3σ standard deviations were found to be 0.83° for α and 0.32° for β.

The SEM cross-section micrograph in **Figure 19** shows an example of the effect of RIE lag on the etching of



**Figure 19**

SEM cross-section micrograph of trenches of different width etched in a DRM system (for eight minutes). The reduced depth of the high-aspect-ratio trenches was due to RIE lag. From [38], with permission.

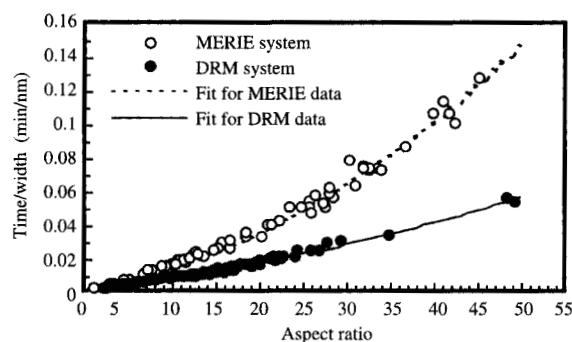
high-aspect-ratio trenches. The effect scales with the trench width  $w$  and is independent of etching time.

The following equation describes the correlation:

$$t/w = \varepsilon A + \rho A^2, \quad (1)$$

with  $A$  being the aspect ratio (depth/width),  $t$  the etching time, and  $\varepsilon$  and  $\rho$  empirically derived parameters [40]. The parameter  $\varepsilon$  is the inverse of the etching rate at  $t = 0$ ; the parameter  $\rho$  quantifies the RIE lag. **Figure 20** shows experimental  $t/w$  data for MERIE and DRM etching systems. The etching rate at  $t = 0$  was 1.08 μm/min for the MERIE system and 1.60 μm/min for the DRM system. In addition to the higher etching rate at  $t = 0$ , the DRM system displayed reduced RIE lag: The parameter  $\rho$  was approximately a factor of 4 smaller for the DRM system. The main parameters controlling RIE lag are the neutral-to-ion flux ratio and the ion-to-inhibitor flux ratio at the bottom of the trench. The reduction of RIE lag in the DRM reactor was caused by a higher degree of etchant-gas fragmentation, leading to an improved neutral-to-ion flux ratio. Higher etching rate and reduced RIE lag ensure productivity improvements, particularly for future trench DRAM generations. Aspect ratios close to 50, depicted in Figures 19 and 20, are not expected to be needed prior to 16Gb DRAM generation products.





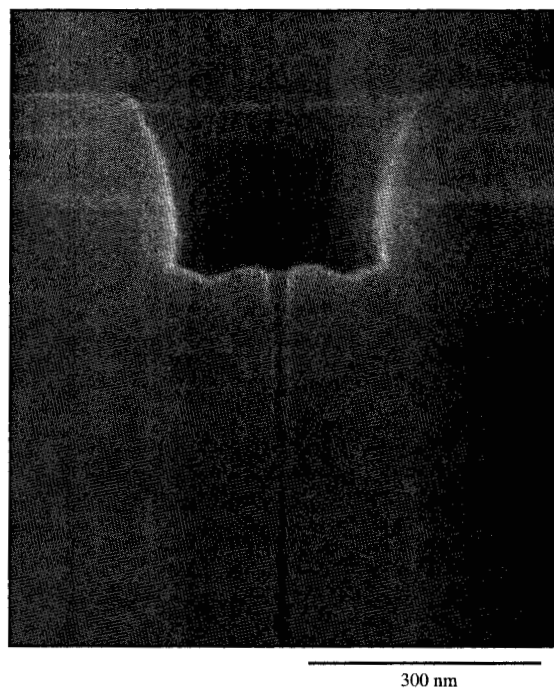
**Figure 20**

RIE lag effects measured for silicon trenches etched in MERIE and DRM systems. From [38], with permission.

### • Silicon recess etching

In a DRAM that utilizes trench storage capacitors, it is imperative to isolate the polysilicon material inside the trench from the transfer device. Also, tighter ground rules necessitate using a buried polysilicon strap to move charge in and out of the storage capacitor. A process is required, therefore, that removes or "recesses" the upper portion of the polysilicon from the trench storage capacitor. For sub-0.25- $\mu\text{m}$  ground rules, three of these polysilicon recesses are required. Polysilicon recesses are also used industrywide in the fabrication of chip interconnections, where studs of polysilicon are recessed in similar fashion to eliminate shorting between metal lines in damascene applications.

The recess etching process can be divided into two parts: local planarization etching and trench recess etching. In the local planarization etching process, the polysilicon film is adjusted to form a uniform, conformal layer over the topography of the substrate created by previously defined contacts or trenches. The goal of the local planarization is to uniformly etch off the polysilicon with a minimal loss of the underlying substrate, thus exposing the top filled trenches in array areas. Local planarization can be employed as a process alternative to chemical mechanical planarization. The locality of the planarization depends upon both the global uniformity of the etching process and the thickness variation of the polysilicon across the chip. The thickness variation, in turn, depends upon the range of the topography and the conformality of the substrate. Therefore, with a highly uniform local planarization etching process, the array will be locally planarized. However, in areas of the chip without trenches (i.e., support regions), the original thickness of the polysilicon is usually larger, so some of

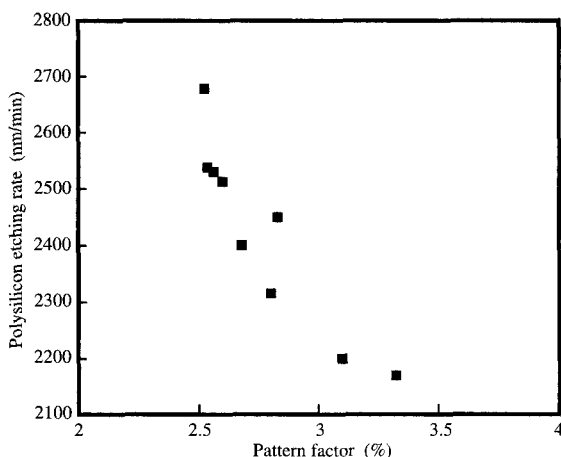


**Figure 21**

SEM cross-section micrograph of a deep trench, revealing a seam which has been preferentially attacked during polysilicon recess etching.

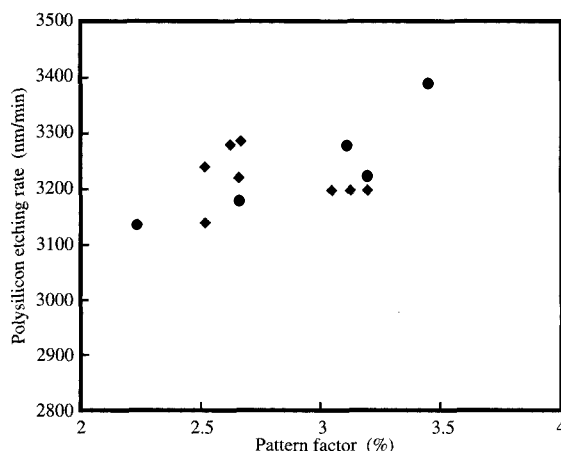
the material being etched remains. During the trench (or contact) recess etching process, the filled trench structures are recessed in order to define a fixed depth below the top of the trench structure. In addition, the polysilicon that was not removed from the surface during the local planarization step is etched and stripped from the surface.

The requirements for a polysilicon recess process entail the need for a high selectivity to the field material (usually nitride or oxide). Since the integrity of the films surrounding the storage nodes is important for subsequent processing, the etching rate or removal rate of the polysilicon must be much higher than those for the surrounding films. Generally, the selectivity of such an etching process should be more than 50 to 1. The polysilicon etching process must also be isotropic. This is necessary to ensure that all of the polysilicon is removed laterally from the sides of the trenches. Since a trench or contact hole is filled by a polysilicon deposition process that leaves some kind of seam as it fills, the recess etching process must be designed so that it does not preferentially attack such a seam (**Figure 21**). This would result in the formation of a void in the polysilicon-filled structure. For this reason, the industry has shunned pure chemical



**Figure 22**

Polysilicon recess etching-rate variation vs. pattern factor (ratio of area of exposed Si to wafer area) for a parallel-plate reactor.



**Figure 23**

Polysilicon recess etching-rate variation vs. pattern factor in an inductively coupled reactor.

downstream etching processes for this application in favor of more traditional RIE techniques, which do not attack these seams as readily. Chemical downstream applications are discussed in more detail later in this paper.

The recess etching process must be uniform across the wafer and across the lot, and the average etching rate should be such that it does not affect cycle time. The process should be free of particulate and metallic

contamination. The wafer-to-wafer uniformity becomes less of a concern if an endpoint technique such as lateral interference interferometry is utilized [41]. In this technique, the depth can be monitored *in situ*; therefore, the etching process can be stopped when the proper depth is obtained. This endpoint technique is important, since the recess etching rate varies with aspect ratio (depth and width of trench) and trench density (silicon load).

The process chosen for such an application usually requires a low-bias-power process using an  $\text{SF}_6$ -based system.  $\text{SF}_6$  is a prolific generator of fluorine that results in the necessary selectivity and isotropy [42–44]. The use of low bias power reduces the dc bias, further increasing selectivity. Still, some amount of ion bombardment is required to minimize redeposition of etching products. The bombardment also prevents pure isotropic etching that would preferentially attack the polysilicon fill seams. Parallel-plate reactors have traditionally been used for this application. However, as aspect ratios and uniformities become greater, the use of inductively coupled plasmas has become appropriate for this purpose. As mentioned earlier, a problem encountered using a standard parallel-plate reactor with an  $\text{SF}_6$ -based system is that etching rates can vary with the silicon load on the wafer. The percent silicon load can change by product design and the critical dimension of the trench profile. Within the trench width specifications, the polysilicon etching rate of the recess can vary extensively, as shown in **Figure 22**. Though the use of an endpoint system mitigates this problem, a process that is minimally affected by the silicon load is more manufacturable.  $\text{SF}_6$ -based processes in inductively coupled reactors are not as sensitive to the problem.

**Figure 23** shows that this recess etching rate variation is much less. This is attributable to the rf reactor design, especially the lower pressures obtainable in these systems. It is expected that uniformity improvements, loading effects, and endpoint control will continue to be the focus of recess etching process development.

#### • Chemical downstream etching

An etching technique complementary to traditional RIE processes that is becoming increasingly popular in the semiconductor industry today is chemical downstream (plasma) etching (CDE). In such etching, the plasma source is generated by a discharge located remotely from the etching region. Only long-lived neutral species are transported to the wafer surface for reaction. Therefore, CDE differs from conventional plasma etching in that ions, electrons, electric and magnetic fields, and the radiation resulting from the plasma are shielded from the wafer surface, ensuring that there is no plasma-induced damage. Additionally, a highly selective etching process which is chemically driven and highly isotropic is attainable. CDE uniformity is achieved by the

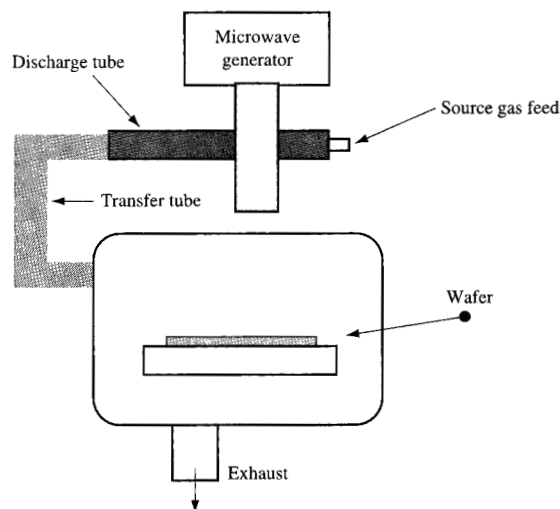
homogenous transport of etchant species rather than the uniformity of the reactive plasma, as is the case in traditional RIE. Finally, downstream etching chambers are covered in a dielectric material to eliminate the possibility of metallic contamination to the substrate being etched.

Horiike et al. [45–47] have demonstrated that CDE can be used to isotropically etch a wide range of materials such as polysilicon,  $\text{Si}_3\text{N}_4$ , resist, polyimide, and refractory materials such as Nb, Mo, and W. By maintaining the wafer at a constant temperature near  $25^\circ\text{C}$ , this dry-etching technique can be utilized to etch substrates with both good uniformity and reproducible etching rates. With CDE, the etching rate of a given substrate can be tuned to the desired value while maintaining an extremely high chemical selectivity. In addition, the process can be easily endpointed by monitoring the extinction of the chemiluminescence above the wafer. The dominant application of this process in semiconductor manufacturing has been in high-selectivity (20:1) etching. One example is the removal of a silicon nitride mask selective to oxide or polysilicon in processes using the local oxidation of silicon (LOCOS) approach [5]. Additionally, CDE is being used for recess etching of high-aspect-ratio features in memory structures.

#### Process description

A schematic of a CDE reactor is shown in **Figure 24**. The reactive species are created by microwave excitation (2.45 GHz) in a discharge tube mounted transversely through a waveguide. Standard process gases include  $\text{CF}_4$ ,  $\text{O}_2$ ,  $\text{N}_2$ ,  $\text{NF}_3$ , and  $\text{Cl}_2$ . A stable afterglow-type plasma can be generated for a variety of gas mixtures and flows. The stability is achieved by a feedback mechanism that minimizes the reflected power back into the microwave cavity.

A significant number of gas species can be produced in the microwave discharge from a typical gas mixture of  $\text{CF}_4$  and  $\text{O}_2$ . Early investigations using mass spectrometry have shown the following species to be present in the discharge:  $\text{CF}_2^+$ ,  $\text{COF}_2^+$ ,  $\text{COF}^+$ ,  $\text{CF}_3^+$ ,  $\text{CO}_2^+$ , and  $\text{O}_2^+$  [45–47]. Of the plasma species generated, only a small number have sufficient lifetimes to reach the substrate that is being etched. The investigations have identified the important role of long-lived  $\text{COF}^*$  and  $\text{O}^*$  (radicals) which are transported to the wafer surface to produce the necessary short-lived F radicals needed for etching. A recent modeling study from the Sandia National Laboratory [48] of the CDE plasma source, which incorporates a comprehensive number of experimental gas-phase cross sections, provides a framework to show the dominant reaction paths for dissociation and ionization of the gaseous species. Results of this model are consistent with other research in this area [49]. Surface chemistry



**Figure 24**

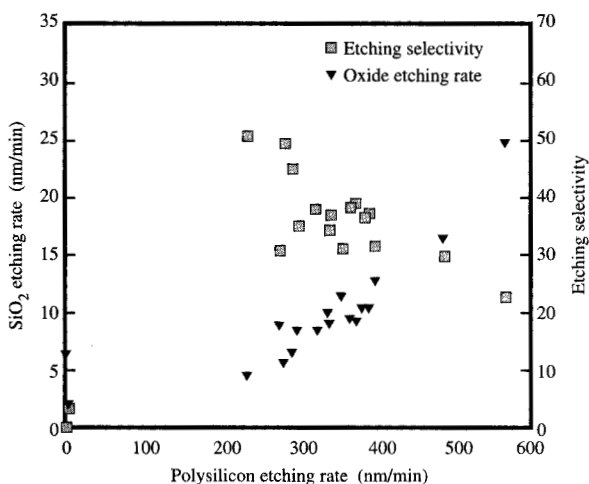
Schematic of a CDE reactor.

mechanisms also affect the etching-rate variations as a function of gas-flow ratio. Nishino et al. [50] have shown that a thick silicon compound layer is formed on the etched surface at high  $\text{O}_2$  concentrations. X-ray photoelectron spectroscopy (XPS) analysis suggests that this layer is  $\text{SiF}_x\text{O}_y$ ; once this layer is formed, the surface deposition limits the available fluorine atoms that reach the Si surface. Oxygen increases the thickness of this layer, and as a result, the Si etching rate is reduced at high  $\text{O}_2$  concentrations.

Another important property of CDE is the control of chemical selectivity. **Figure 25** shows the etching rate and subsequent etching selectivity of polysilicon with respect to  $\text{SiO}_2$  over a wide range of parameters such as gas flow and pressure. Using CDE, the etching rate of polysilicon can be varied over a wide range; the chemical selectivity to oxide remains high because of the large difference in polysilicon and oxide bond energies.

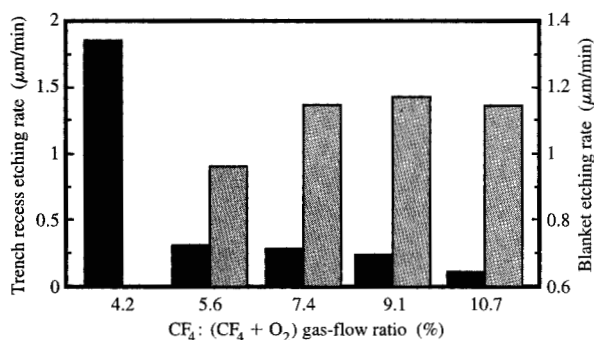
#### Applications

CDE can be effectively integrated into semiconductor etching applications that require one or more of the following capabilities: a highly uniform blanket etching process or etch-back; minimum plasma damage; or an isotropic, high-selectivity-to-oxide etching process. CDE can perform these applications reliably by accurately endpointing the amount of over-etching for a substrate; controlling selectivity and rate by a factor of 5 to  $10\times$  by adjustable tool parameters; providing a stable rate and selectivity; and integrating real-time thin-film process



**Figure 25**

SiO<sub>2</sub> etching rate (inverted triangles) and etching selectivity of polysilicon with respect to SiO<sub>2</sub> (squares) as a function of polysilicon etching rate, for a CDE reactor.



**Figure 26**

Trench recess etching rate (dark bars) and blanket etching rate at several gas-flow ratios. The etching was carried out in a CDE reactor.

control (by ellipsometry or interferometry) into the processing environment.

Process applications of CDE commonly utilized for semiconductor processing can be separated into the following three types: recess etching, strip, and soft silicon etching. Nitride-selective-to-oxide stripping [51, 52] and soft silicon etching [50] have been covered in the referenced studies; the interested reader is referred to those studies for relevant information.

Historically, CDE systems have been used to etch large surface areas with minimal aspect ratios; thus, loading effects through which the rate can dramatically change with varying surface areas are minimal [53]. The etch-back or recess of substrates within a high-aspect-ratio structure presents some unique challenges. Under these conditions, loading effects can have a severe impact on the ability to control both the uniformity and magnitude of the etched depth across the wafer. In addition to classical loading, etching rates that depend on the aspect ratio are found (i.e., RIE lag), and can complicate the trench recess process.

In a 0.25-μm trench DRAM process, resist etchback is required as part of storage-node formation [3]. Because resist coating does not leave voids and requires isotropic removal, CDE is an ideal application for this level.

Figure 26 shows the recess and blanket resist etching rates over a range of CF<sub>4</sub>:(CF<sub>4</sub> + O<sub>2</sub>) gas-flow ratios (CF<sub>4</sub> flow rate divided by the sum of CF<sub>4</sub> and O<sub>2</sub> rates) in percent. The blanket rate is found to increase from 0.85 to 1.15 μm/min with increasing fluorine concentrations, over the range of 4.2 to 10.7%. The rate is fluorine-reactant-limited. We note that for the case in which only O<sub>2</sub> is introduced into the plasma, no resist removal can be measured in a CDE tool, since a relatively low wafer-surface temperature is maintained. The chemical selectivity of resist to a blanket film of TEOS over the indicated range of gas-flow ratios is >100:1. If the same etching conditions are applied to a 0.25-μm-nominal-width resist-filled deep trench (>3 μm) which is lined with a TEOS-deposited layer, the depth from the top of the trench, determined at a fixed etching time, varies from 1.82 to 0.7 μm. This corresponds to a rate varying from approximately 1.88 to 0.13 μm/min, as also shown in Figure 26. Since the trench recess etching rate decreases with increasing percent gas-flow ratio, the rate is not limited by fluorine concentration. For the lowest gas-flow rate of fluorine (4.2%), the rate increases from the blanket etching process to the trench recess etching process, from 0.85 to 1.82 μm/min, respectively, corresponding to a decrease in the etched volume per unit time. The classical loading effect is operational for this case only. At larger fluorine concentrations, the trench recess etching rate behavior is not fluorine-limited and cannot be explained by loading.

An examination of the trench resist recess depth as a function of etching time, plotted in Figure 27 as a function of aspect ratio for flow rates of 3 and 7.5%, reveals two distinct etching behavior patterns. At low recess aspect ratios (i.e., <5), for both fluorine concentrations, the etched depth is linear with time, and the larger rate in the trench compared to the blanket resist rate can be explained by classical loading. An etched depth saturation is found for the case of the higher fluorine concentration, while the behavior for the lower

fluorine concentration remains linear. Use of the latter can extend the recess to quite high aspect ratios. Analysis of SEM cross sections at the longest etching times (80 s) showed the formation of a thin film above the recessed resist only for the case of the higher fluorine concentration. Studies of the dependence of the resist recess etching rate aspect ratio on wafer temperature, pattern factor variation, trench width variation, and buffer gas addition have also been carried out.<sup>6</sup>

A mechanism for aspect-ratio dependence can be developed from the cumulative evidence. As the resist material is etched, F radicals degrade the polymer structure and O radicals volatilize, forming CO, CO<sub>2</sub> by-products. In a highly O<sub>2</sub>-rich CF<sub>4</sub>/O<sub>2</sub> gas flow, a COF<sub>x</sub> layer may be formed on the resist surface. Slightly higher fluorine concentrations may trigger an enhanced formation rate and/or a more stable form of the COF<sub>x</sub> layer. Once the resist surface within the trench forms the COF<sub>x</sub> layer, the resist can be etched only by F and O radicals through this deposition layer. This implies that the resist recess etching rate depends on the thickness of the COF<sub>x</sub> layer. The transition from a constant rate at low aspect ratios to an etch-stop regime may indicate that the COF<sub>x</sub> layer is of sufficient thickness to slow down and subsequently stop the etching process. Perhaps the formation of the COF<sub>x</sub> layer only on the resist surface and not on the sidewalls of the TEOS may be due to the differences in the equilibrium vapor pressure, because of preferential deposition at higher vapor pressure on the positive curvature resist surface compared to the vertical sidewalls. The proposed mechanism is similar in nature to the mechanism for silicon surface smoothing by deposition of SiF<sub>x</sub>O<sub>y</sub>, advanced by Nishino et al. [50].

In summary, a new application of chemical dry etching has been shown to etch high-aspect-ratio resist structures. CDE aspect-ratio-dependent etching behavior is extremely sensitive to the CF<sub>4</sub>/O<sub>2</sub> gas-flow ratio. At low fluorine concentrations, a constant etching rate can be achieved, and classical loading occurs. At high fluorine concentrations, at an aspect ratio of approximately 5, saturation occurs, producing etch-stop behavior for long etching times. A CDE process taking advantage of this behavior has been used for resist recess applications in DRAM process sequences.

#### ◆ Gate-conductor etching

Gate-conductor etching of linewidths of 0.25 μm and below has introduced new challenges. The need to control the etched profile, etching selectivity, and overall critical dimension (CD) is the driving force behind these challenges. In the majority of gate-conductor applications, there are two aspects of dry etching to consider: the

<sup>6</sup> S. Halle, unpublished results.

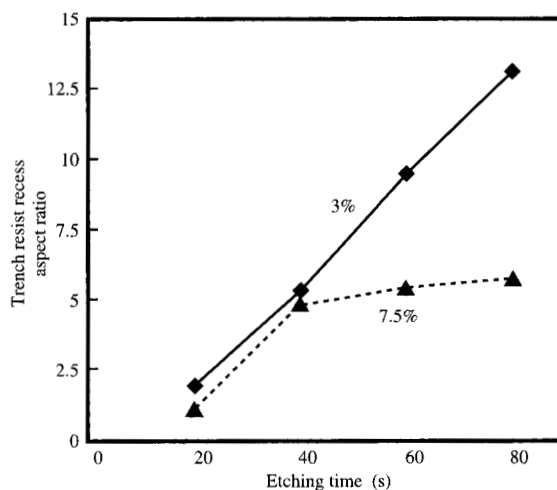


Figure 27

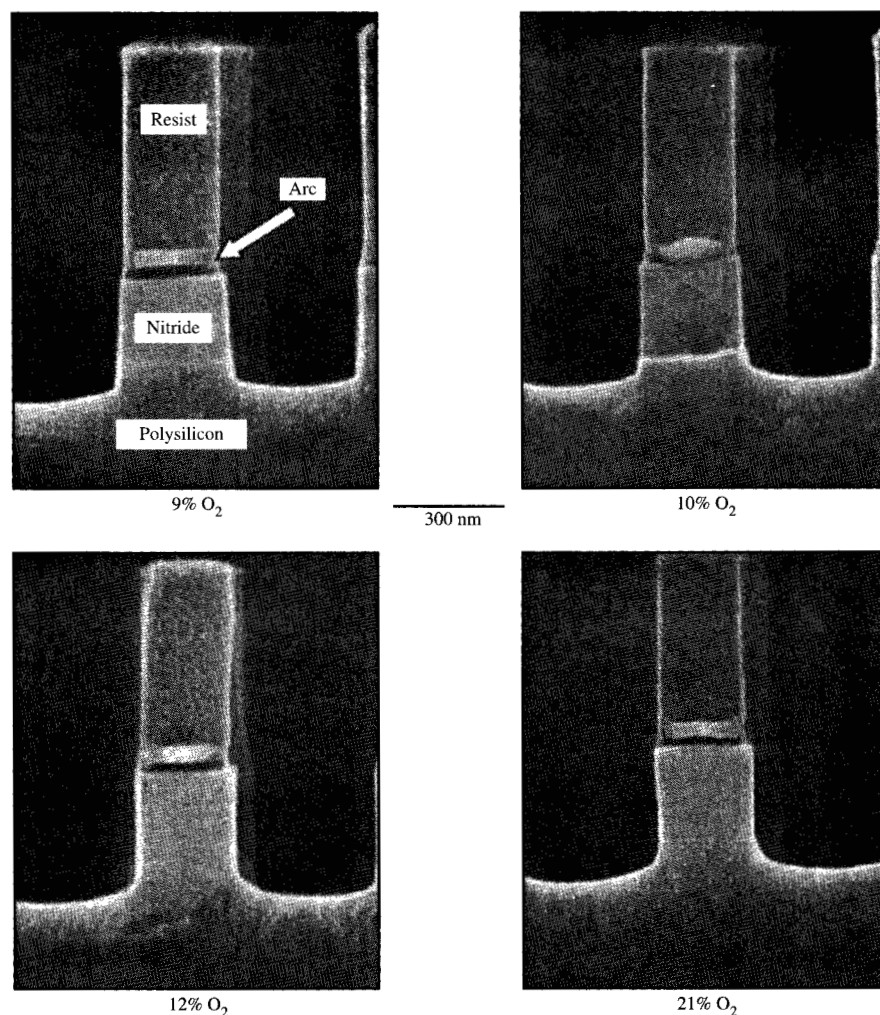
Trench resist recess etch depth as a function of etching time and aspect ratio.

formation of the mask which defines the gate-conductor pattern and the etching of the conductor films themselves.

The photolithographic pattern can be used solely as the pattern-transfer mechanism for the gate-conductor films, eliminating the need for mask formation. However, the use of a hard mask for both memory and logic gate-conductor formation is becoming more widespread in the semiconductor industry.

For logic devices, the main parameter to control is the gate-conductor critical linewidth, which defines the speed of the devices [54]. The principal gate-conductor thin film is polysilicon. For memory devices, the majority of manufacturers utilize a compound gate stack of tungsten silicide (WSi<sub>x</sub>) and polysilicon. A compound gate conductor incorporates polysilicon and an additional film that serves to lower overall conductor (wire) resistivity (to improve memory performance). With the addition of a second material into the gate conductor, the complexity of the dry-etching process is significantly increased. The gate level in semiconductor fabrication was one of the first for which ICP reactors were used to achieve improved dry etching.

As devices are scaled in size horizontally, they must also be scaled vertically to keep physical and electrical tolerances within design limits. Wiring capacitance between adjacent gate-conductor lines increases with aspect ratio. Also, as the aspect ratio increases, it becomes more difficult to fill the space between the gate conductors with an isolation dielectric. Thinning the gate conductor reduces the aspect ratio. For the 0.25-μm generation, the gate-conductor film thicknesses are less than 0.20 μm [3].



**Figure 28**

SEM cross-section micrographs illustrating gate-conductor hard-mask etching at several percentages of oxygen in the total gas flow. As can be seen, the mask fabricated using 9%  $O_2$  had a profile with a positive slope; the one fabricated using 21%  $O_2$  had a significant reentrant angle.

ICP etching is used for its process control benefits rather than its high-etching-rate aspects in order to reliably etch these thinner gate conductors.

#### *Gate-conductor mask open (GCMO) reactive ion etching*

For some gate-conductor applications, resist is used as a "soft mask" to define the gate conductors. Alternatively, it is used as an intermediary in the formation of a hard mask. Hard masks are normally composed of a dielectric such as silicon dioxide ( $SiO_2$ ) or silicon nitride ( $Si_3N_4$ ). The use of a hard mask allows the removal of the resist prior to the etching of gate conductors, thus preventing the by-products of the resist erosion from affecting the

etching. Additionally, the hard-mask film can be utilized for other levels of device integration that follow the formation of the gate conductors, such as self-aligned contacts (SACs). However, utilizing a soft mask has both cost and process simplicity advantages.

For 0.25- $\mu m$  dimensions and below, deep-UV photolithography equipment (248 nm) and resist systems are needed. Also, to reduce the degree of substrate reflectivity, an organic or inorganic antireflective coating (ARC) can be utilized. The ARC material is normally applied to the gate-conductor thin films prior to resist application. If an ARC is used, it must be etched prior to the dry-etching formation of the gate-conductor mask.



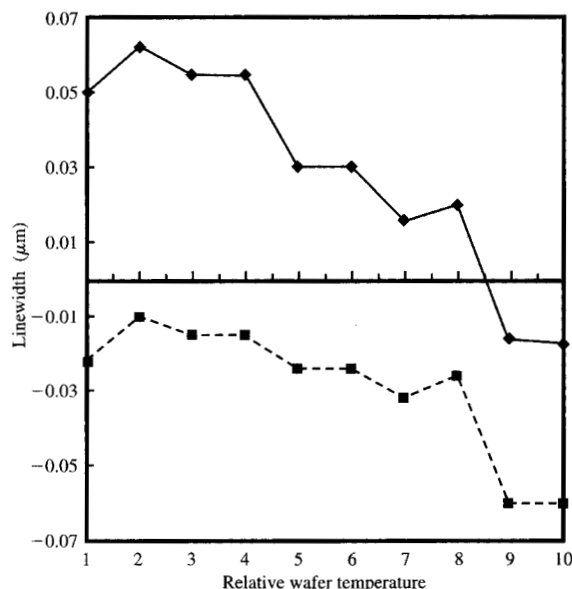
When utilized, the ARC must be considered part of the overall hard-mask process and must satisfy hard-mask requirements.

The most critical aspect of the gate-conductor mask-etching process is control of the gate-conductor critical dimension (CD). This critical dimension is the gate length that defines the final performance of the device [54]. Gate linewidth variations include across-chip linewidth variations (ACLVs), across-wafer linewidth variations (AWLVs), and lot-to-lot variations. Additionally, there are variations of the gate-conductor etching process caused by the local pattern density. Within the same local environment on a chip, the gate conductors can be patterned either in a tightly spaced array, designated as "nested lines," or as "isolated lines." The gate-conductor linewidths for nested and isolated lines vary because of a combination of effects. These effects include optical inconsistencies in the lithography tools and photoresist as well as nonuniformities in the etching equipment [6]. (The combination of all of the above-mentioned effects is referred to as the total CD bias of the gate conductor.)

A hard mask must replicate its resist pattern without dimensional changes. Fluorinated chemical systems are commonly used in the plasma etching of dielectric hard masks [55]. The amount of polymerization in these systems during etching is the determining factor in CD control. Also, the uniformity with which the etching equipment generates the polymer is critical. Polymer formation generated by a reactive ion etching plasma has been the focus of many studies [26, 56]. Excessive polymer formation tapers the transferred pattern, resulting in a linewidth increase. If the plasma produces too little polymer, the sidewall of the etched profile is unprotected and etches laterally, causing a re-entrant or negatively sloped profile. **Figure 28** shows an example of the effects of plasma composition on profile. These wafers were processed using a conventional fluorinated gas mixture with oxygen flow adjustments.

Besides controlling polymer formation in the plasma, the design of the plasma-etching reactor can affect CD control as well. Intrinsic deficiencies in reactor hardware and/or design affect the way the polymer is distributed and deposited across a wafer. As an example, temperature plays a crucial role in the control of the GCMO CD. Wafer temperature nonuniformities caused by poor design of wafer chucks can severely affect polymer deposition. Higher temperatures typically reduce the amount of polymer that remains on etched surfaces. Temperature changes as small as 20°C can result in linewidth variation. In an attempt to quantify the effects of polymer formation and its impact on CD control, a study was made of a Si<sub>3</sub>N<sub>4</sub> GCMO hard mask for 256Mb DRAM applications.<sup>7</sup>

<sup>7</sup> P. D. Hoh et al., IBM, Hopewell Junction, NY, unpublished results.



**Figure 29**

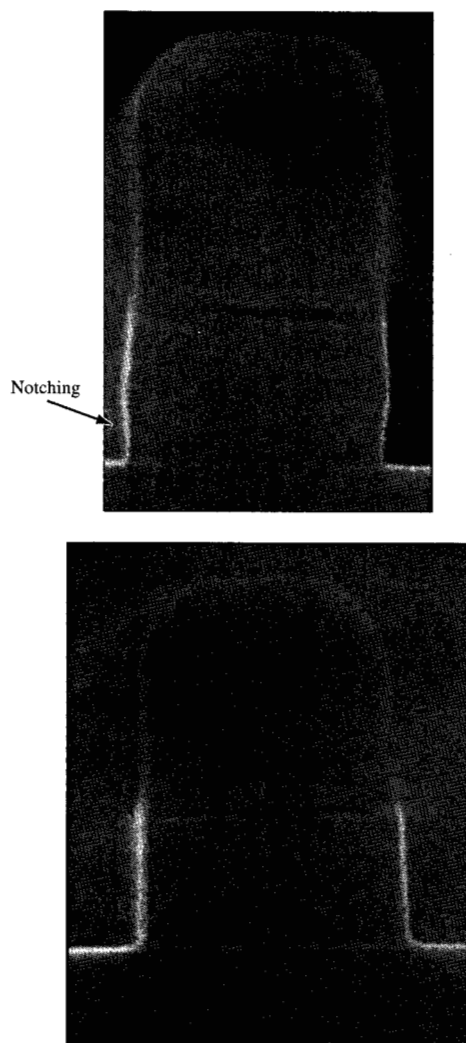
Illustrative effect of wafer temperature during hard-mask etching on critical linewidth of isolated (solid line) and nested (dashed line) GC lines.

Patterned GCMO wafers were each etched at electrode temperatures ranging from 15° to 60°C. Each wafer was etched under identical conditions, with the etching being terminated by an optical emission endpoint system. An etching process consisting of CF<sub>4</sub>/CHF<sub>3</sub> and a MERIE etching system were used for this experiment. Wafers were held in thermal contact with the electrode by means of a mechanical clamping system. Because of the minimal thermal contact thus achieved, it was recognized that wafer temperature would be significantly higher than what was measured and controlled in the circulating cooling liquid. The critical linewidth for each wafer was then measured utilizing an electrical linewidth test circuit. Test algorithms were used to calculate linewidths from the measured wire resistivities. **Figure 29** illustrates the effects of relative wafer temperature on linewidth. The data indicate that the linewidth bias decreases with increasing wafer temperature.

#### Gate-conductor stack etching

For CMOS devices, use is made of polysilicon [56, 57] gates. After patterning, the polysilicon is doped with an impurity, such as phosphorus, to make it electrically conductive. The polysilicon must be patterned without significant attack of the underlying gate oxide. As in the





**Figure 30**

SEM cross-section micrographs of 0.20- $\mu\text{m}$ -wide polysilicon logic gates etched with both standard flow rates (top) and high flow rates (bottom) of HBr. Note the reduction in notching at the base of the polysilicon gate with the increase in flow rate.

**Table 4** Gate-oxide thickness for several device generations.

| Device generation<br>(minimum gate-<br>conductor width)<br>( $\mu\text{m}$ ) | Gate-oxide thickness |               |
|------------------------------------------------------------------------------|----------------------|---------------|
|                                                                              | Memory<br>(nm)       | Logic<br>(nm) |
| 0.35                                                                         | 10                   | 4.5           |
| 0.25                                                                         | 8                    | 3             |
| 0.18                                                                         | 6                    | 2.5           |
| 0.15                                                                         | 5                    | 2             |

GCMO, the stack etch process must not change the critical dimension of the etched feature. These processes use gases such as  $\text{Cl}_2$ , HBr, or HCl to provide chemical selectivity to the gate oxide.

To advance logic and memory device performance, both the gate-conductor linewidth and the gate-oxide thickness are being reduced (see **Table 4**). These two parameters are being reduced more aggressively in logic than in memory applications [54]. Traditionally HBr gas has been used to etch polysilicon gate conductors with a high selectivity to gate oxide and acceptable profile control. As minimum gate-conductor widths have fallen below 0.25  $\mu\text{m}$ , the need for an improved HBr-based plasma-etching-process performance has been recognized.

Several challenges had been identified in the use of HBr-based systems in a conventional plasma reactor. To achieve the highest possible etch performance, operation at both low bias power and low pressure was necessary. The use of low bias power reduced the degree of plasma damage to the thin gate oxides but severely lowered the polysilicon etching rate; the low pressure was needed to achieve stringent linewidth control, resulting in plasma instability in the conventional reactor.

To achieve both low pressure and low bias power etching, use was made instead of an ICP reactor, making it possible to control wafer bias power independently of plasma source power and providing reasonable etch rates at the very low ion energies necessary to avoid gate-oxide damage. Stable operation could be achieved at pressures as low as 2 mTorr and wafer bias powers of 50 W. Concurrent with the use of the ICP system, it was determined that a short-gas-residence-time (SGRT) [58] plasma-etching process was also needed. SGRT etching uses large flows of reactant gas (>200 sccm), in this case HBr, at pressures below 10 mTorr. This technique increases the availability of neutral etchant species and reduces the concentration of reaction products in the plasma. The latter effect helps to minimize pattern density effects (e.g., microloading). SGRT also improves profile control by eliminating polysilicon notching at the gate oxide/polysilicon interface, as shown in **Figure 30** [59].

**Figure 31** shows a plot of the etching rate of polysilicon vs. total gas flow for both  $\text{Cl}_2$ - and HBr-based etching processes. In the 75–150-sccm flow range for a  $\text{Cl}_2$ -based system, the etching rate is limited by the reactant supply to the wafer surface. As can be seen, at  $\text{Cl}_2$  gas flows of 200 sccm and greater, the etching rate saturated at the rate of ion-assisted reactions (i.e., ion flux). At all of the chlorine flow rates examined, the degree of photoresist erosion and selectivity to the gate oxide were unacceptable for sub-0.25- $\mu\text{m}$ -generation devices. In the case of HBr-based systems, no change in etching rate was observed with increasing flow rate, suggesting that the HBr-based

etching process is limited by the surface reaction rate rather than by the flux to the surface.

Microloading is one of the main mechanisms for critical dimension differences between features. Localized microloading is evident when the critical dimension of nested and isolated lines varies within the same design size. The width difference between nested and isolated structure critical dimensions ( $\Delta$ ) can be used as a global quantitative measurement of profile microloading. When a SGRT etch is utilized, it provides a dramatic increase in etching species and the effective evacuation of reaction products. High-flow processing with HBr-based systems helps eliminate the uneven distribution of etchants at the wafer surface, improving  $\Delta$ .

Conventional low-flow processes yielded a value for  $\Delta$  of 0.03  $\mu\text{m}$ . When the flow rate of HBr was increased to 150 sccm (at 8 mTorr), the value for  $\Delta$  at the wafer edge improved to 0.01  $\mu\text{m}$ . Any further flow increase overwhelmed the pumping capability of the reactor system, and pressure-induced microloading became the dominant effect. By improving the pumping efficiency of the system, higher flow rates and lower pressures were possible. An additional reduction in  $\Delta$  was achieved by reducing the aspect ratio of the pattern via the photoresist mask thickness (from 0.80  $\mu\text{m}$  to 0.50  $\mu\text{m}$ ). With total HBr gas flows of  $\geq 225$  sccm, pressures less than 5 mTorr and smaller pattern factors, the value of  $\Delta$  across the wafer could be reduced to 0.008  $\mu\text{m}$ . The resulting profile improvement of the gate conductor with SGRT etching can be seen in Figure 30.

With the introduction of ICP sources for gate-conductor etching, a reduction in gate plasma damage [2] to beyond detectable limits has been obtained. Table 5 lists a variety of RIE plasma chamber types and the corresponding yields of large-area antenna structures used to detect plasma-induced charging. The charge monitors are large areas of gate conductor which collect charge generated by the plasma-etching process. These antennas are then connected to a relatively small grounded electrode across a thin gate oxide. By varying the size of the antenna to grounded electrode area, the amount of plasma-induced charging can be estimated.

Compound GC stacks have been used in various generations of memory products. Figure 32 shows several illustrative cross sections of compound GC stacks, consisting of  $\text{WSi}_x$  and polysilicon, by memory generation. Etching processes containing mixtures of HCl and  $\text{Cl}_2$  [60, 61] have been shown to reduce the etching rate of polysilicon while the etching rate of  $\text{WSi}_x$  remains unchanged, allowing control of selectivity between the two films. Compound gate-conductor stack films etched using this gas mixture have been found to yield superior performance. Figure 33 shows the effect of etching rates and selectivity as the HCl flow rate is increased.

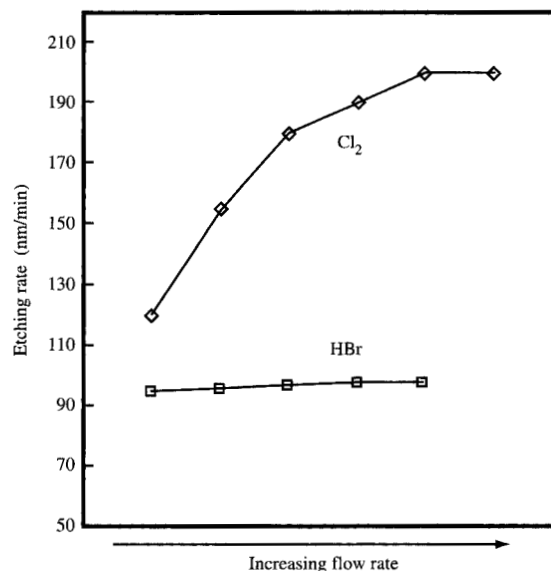


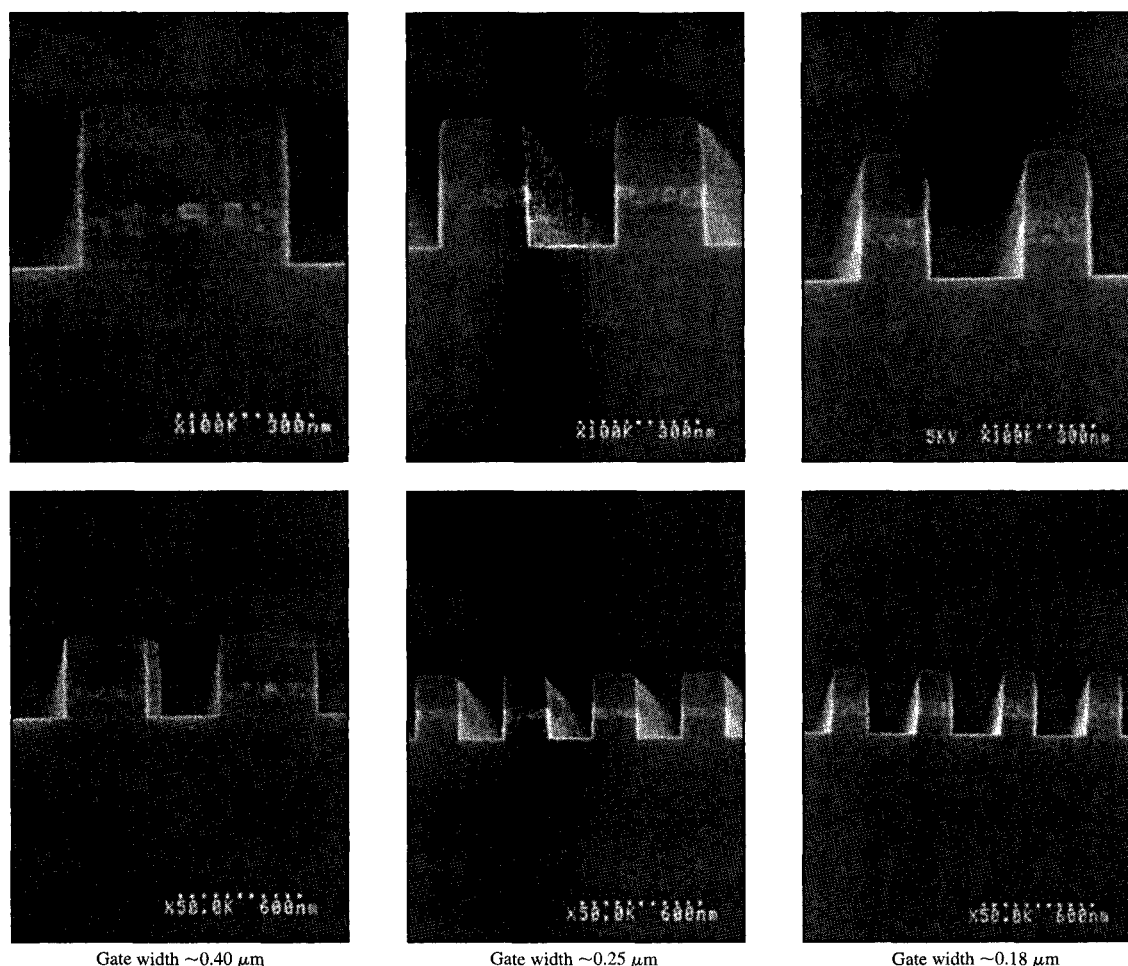
Figure 31

Polysilicon etching rate for HBr- and  $\text{Cl}_2$ -based systems vs. flow rate.

Table 5 Yields of large-area antenna structures used to detect plasma-induced charging, for different types of RIE reactors.

| Reactor type                 | Magnet description    | 300K:1 | 1M:1 | 10M:1 |
|------------------------------|-----------------------|--------|------|-------|
| MERIE A                      | Electro-              | 50     | 30   | 20    |
| MERIE A<br>(without magnets) | Electro- (disabled)   | 100    | 100  | 100   |
| MERIE B                      | Permanent             | 80     | 50   | 35    |
| MERIE C                      | Alternating permanent | 88     | 85   | 63    |
| ICP                          | None                  | 100    | 100  | 100   |

The main selectivity concern of traditional gate-conductor etching is the selectivity of doped polysilicon films to the gate oxide. Gate oxides having thicknesses of 0.005  $\mu\text{m}$  must be preserved while etching  $\text{WSi}_x$ /polysilicon films as thick as 0.20  $\mu\text{m}$ . The polysilicon:gate oxide selectivity must be sufficient to allow for complete removal of the polysilicon without etching through the underlying oxide layer. Any residual polysilicon will create leakage pathways, leading to shorted gate-conductor wiring. As gate-oxide thickness are reduced to below 0.01  $\mu\text{m}$ , the thickness of the remaining gate oxide following all of the GC etching and cleaning steps is the preferred parameter



**Figure 32**

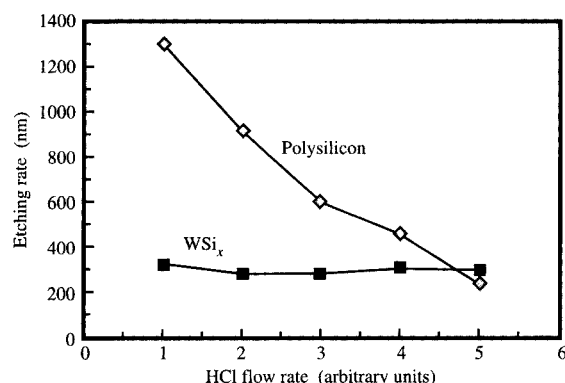
SEM cross-section micrographs of compound gate stacks from several DRAM generations. Etching was carried out in an ICP reactor using a  $\text{HCl}/\text{Cl}_2$  gas mixture.

for characterizing GC patterning performance. This value can be measured and compared directly to device performance and yield.

In sub-0.25- $\mu\text{m}$  generations, selectivity to stack films is as important as selectivity to gate oxide. Plasma-etching processes must allow *in situ* selectivity adjustment as the gate materials are etched. Etch selectivity to the gate mask material is critical. Selectivity to the materials within the compound stack is also important. **Figure 34** illustrates the selectivities needed during compound GC stack etching. For example, if use is made of a hard mask of  $\text{Si}_3\text{N}_4$  for the gate stack definition, the mask is not sacrificial, as is the case with resist, since it is needed as a mask during a subsequent self-aligned contact (SAC) process [4].

Any loss of  $\text{Si}_3\text{N}_4$  during the GC level forces a higher selectivity requirement for the SAC plasma-etching process. When etching  $\text{WSi}_x$  in the GC process with selectivity to oxides greater than 15:1, residual films may be left on the wafer. Often described as "RIE grass," these result from micromasking by oxides incorporated into the  $\text{WSi}_x$  film (**Figure 35**). The high selectivity to oxide processes required for removing the polysilicon films from gate oxide are therefore undesirable for etching of compound gate-conductor films.

Many processing levels occur before the definition of the gate conductor, and can affect the GC etching process. Device isolation is normally achieved by forming an



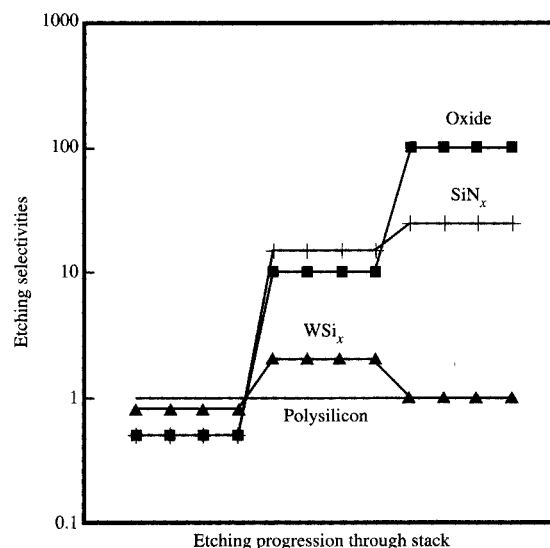
**Figure 33**

Polysilicon and WSi<sub>x</sub> etching rates for HCl/Cl<sub>2</sub> ICP RIE as a function of HCl flow rate.

insulating film between electrically active areas on the wafer. Even with modern isolation techniques, such as shallow-trench isolation (STI), some degree of surface topography exists on the wafer. If the topography is large compared to the GC film thickness, the ability to remove the gate-conductor films completely during the plasma-etching process is affected primarily by the planarizing nature of a conformally deposited film. As a result, the thickness of the GC polysilicon varies with topography, requiring additional over-etching of the polysilicon. This increased over-etching requirement increases the requirements for high selectivity to gate oxide. Illustratively, **Figure 36** depicts a compound GC line passing over topography.

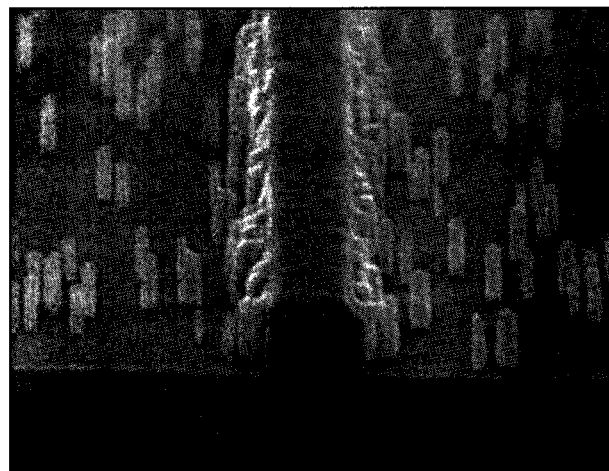
To demonstrate the effects of topography on the gate-conductor etching process, steps of SiO<sub>2</sub> were patterned on several wafers. A compound gate-conductor layer of WSi<sub>x</sub> and polysilicon was deposited on the wafers. A typical GC pattern was then exposed on the wafers, and the gate conductors were etched in two different processing chambers. **Figure 37** depicts the effects of 50- and 100-nm steps of topography on the wafers. Gate-conductor yield loss can be seen for a step as small as 0.05 μm. A topography-modeling program written by Horak et al.<sup>8</sup> can be used to estimate the plasma-etching conditions that are needed for patterning compound gate conductors over topography. **Figure 38** is an example of the process selectivity needed for etching a 0.08/0.08-μm WSi<sub>x</sub>/polysilicon stack over an 0.080-μm step.

<sup>8</sup> D. Horak, unpublished results.



**Figure 34**

Changes in etching selectivities needed during RIE of a hypothetical gate stack.



**Figure 35**

SEM micrograph illustrating micromasking resulting from a high selectivity to oxide during the etching of polysilicon.

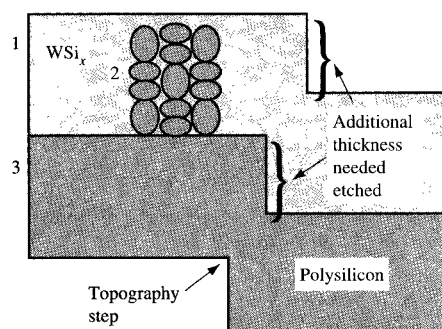
- *Etching of interconnection conduction layers*  
The current challenge in the etching of metal layers to form on-chip wiring is extendibility to sub-0.25-μm

### Interfaces

- 1) Hard-mask/ $\text{WSi}_x$
- 2)  $\text{WSi}_x$  grain boundary/voids
- 3)  $\text{WSi}_x$ /polysilicon

### Topography

- Step height "adder" to etching times
- Compound stacks increase process complexity



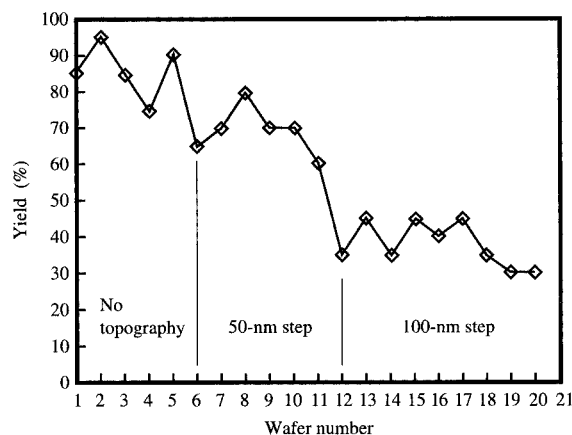
**Figure 36**

Topography and selectivity effects that must be considered when etching a compound gate structure. The SEM cross-section micrograph shows a gate structure as it passes over a topography step.

**Table 6** Typical plasma-etching requirements for Al(Cu)-based wiring at the 0.25- $\mu\text{m}$ -ground-rule level.

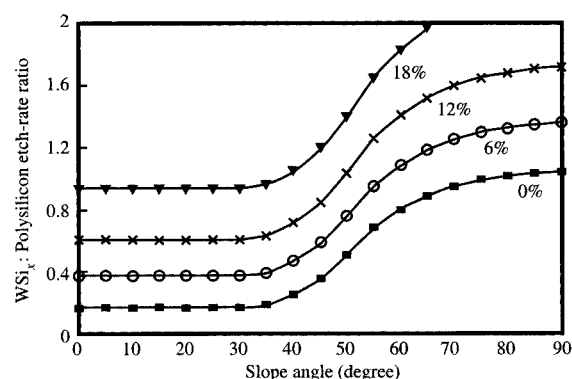
| Parameter                                                | Requirement                    |
|----------------------------------------------------------|--------------------------------|
| Profile                                                  | $>86^\circ$                    |
| Overall resist selectivity<br>(incl. Ti/TiN + over-etch) | $>1$                           |
| Al(Cu) etching                                           | 700–1500 nm/min                |
| Oxide loss                                               | $\sim 20$ nm (in dense arrays) |
| Lateral erosion                                          | None                           |
| Residue                                                  | None                           |
| Etch bias                                                | Controllable                   |
| Corrosion resistance                                     | 72 hr                          |

linewidths. **Table 6** lists typical plasma-etching requirements for 0.25- $\mu\text{m}$ -ground-rule wiring composed of



**Figure 37**

Effects of topography on gate-conductor yield with respect to shorting, indicating more shorting with increasing topography.



**Figure 38**

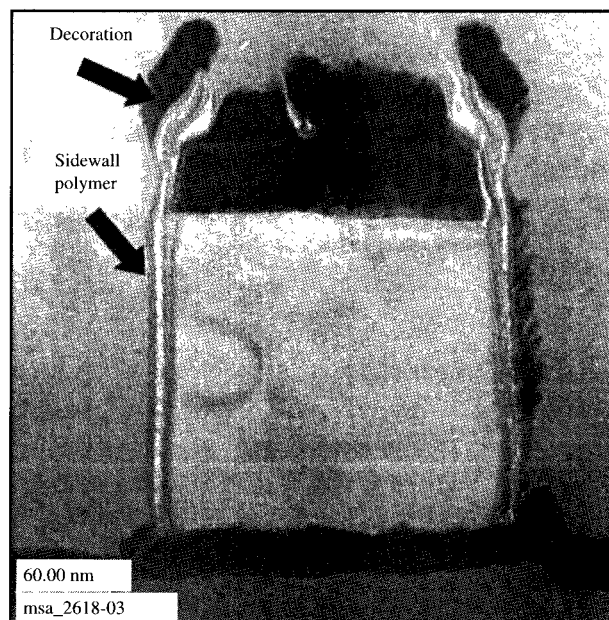
Plot generated by an RIE topography-simulation program showing the amount of etching selectivity needed to successfully etch a specific gate-conductor stack. For this example, a 0.08- $\mu\text{m}$ -thick  $\text{WSi}_x$  film and a 0.08- $\mu\text{m}$ -thick polysilicon film were chosen with a topography step height of 0.08  $\mu\text{m}$ . The slope angle of the underlying topography was assumed to range from 0 to 90°. The various curves indicate the effect of increasing amounts of nonuniformity on the wafer.

Al(0.5% Cu) that is usually capped with barriers or liners consisting of Ti or TiN. These barriers/liners must also be etched as a part of the metal-etching processes used to etch the Al(Cu). Two critical aspects of the processes are corrosion prevention of the metal wires after etching and profile control during etching.

### Corrosion prevention and profile control

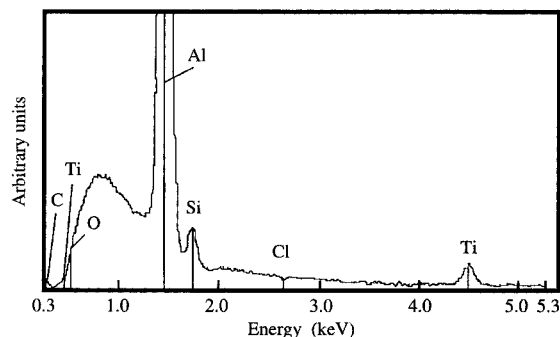
The prevention of corrosion is the most important aspect of on-chip metallization-layer etching. The chemical system typically used to etch the metallization layers is also responsible for the corrosion of the resulting wires [62–64]. The most widely used metal etchant source gases are  $\text{BCl}_3$  and  $\text{Cl}_2$ . The basic mechanism of corrosion is believed to be the conversion of  $\text{AlCl}_3$ , one of the etch by-products, into  $\text{Al}(\text{OH})_3$  and  $\text{HCl}$  [64].  $\text{HCl}$  attacks the sidewall passivation layers and corrodes the metal wires. In addition, alloys of Al and Cu form a galvanic coupling that can accelerate corrosion reactions. Al etching therefore requires a dedicated post-etching cleaning chamber integrated into the plasma reactor. Typically, the remaining resist on the wafer is removed in this additional chamber, without prior exposure of the wafer to atmosphere, with an  $\text{H}_2\text{O}/\text{O}_2$  plasma “ashing” process. Any chlorine that had been absorbed in the photoresist is then removed under vacuum. At the same time, chlorine that had been adsorbed directly on the aluminum is replaced by oxygen. At this point, the metal features on the wafer still have a polymerlike film on their vertical sidewalls, which typically protrudes above the top surface to form so-called “fences” or “rails.” This layer may contain residual chlorine and must be removed using an additional chemical cleaning step. **Figure 39** shows a TEM cross-section micrograph of an Al(Cu) wire after etching in a  $\text{Cl}_2/\text{HCl}$  plasma, resist ashing, and rinsing in water. Most severe corrosion problems can be solved with an integrated plasma-stripping chamber. Any other corrosion occurrences can be minimized by implementing post-wet-etching steps with time-limited steps between metal RIE and post-wet-etching steps. Another approach to preventing corrosion is by addition of  $\text{CF}_4$  to the plasma during post-etching polymer removal. It is believed that Cl radicals that are trapped in the sidewall are replaced by F radicals, effecting a more efficient removal of C, Si, Ti, Al, and  $\text{O}_2$  species incorporated in the polymer. This can be seen in the energy-dispersive X-ray (EDX) spectrum shown in **Figure 40**. The effectiveness of  $\text{CF}_4/\text{O}_2$  plasma for passivation stripping has been studied by Brusich et al. [64].

Despite efforts to prevent gross corrosion, the pitting of Al(Cu) line sidewalls by the etching by-products can still occur. Pitting, known as “mouse bites,” is more easily tolerated when the lines are  $0.5\text{ }\mu\text{m}$  wide; in that case, a mouse bite consumes only a small percentage ( $\sim 10\%$ ) of the cross section of a line. When the line is about  $0.2\text{ }\mu\text{m}$  wide, the mouse bite can consume 25% of the wire cross section, causing failures. **Figure 41** is an SEM micrograph showing an example of a mouse bite. Alternate etchants have been proposed in recent years to minimize corrosion. For example, the use of  $\text{HCl}$  in place of  $\text{BCl}_3$  has been reported to reduce the amount of corrosion [65, 66].



**Figure 39**

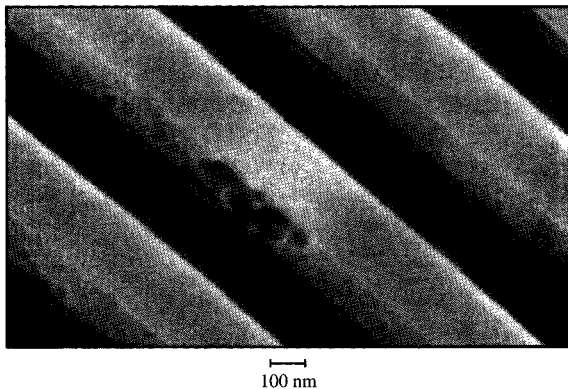
Transmission electron microscopy (TEM) cross-section micrograph of an Al(Cu) wire after etching in a  $\text{Cl}_2/\text{HCl}$  plasma followed by resist ashing and rinsing. Note the remaining “fences” or “rails.”



**Figure 40**

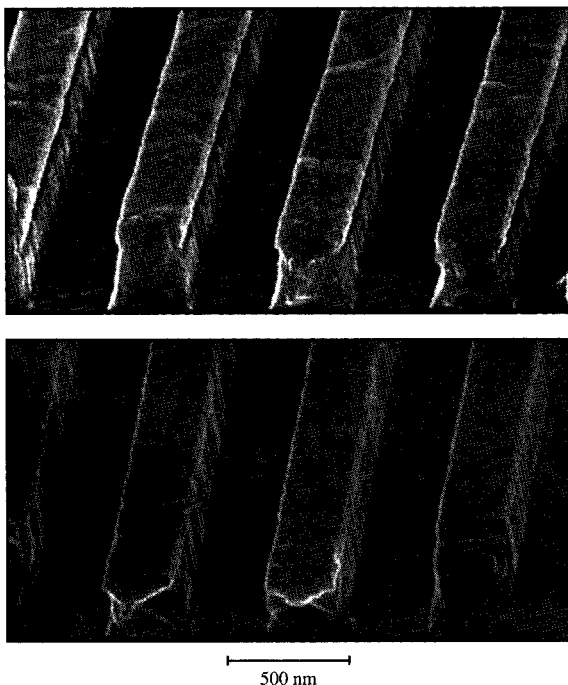
EDX characteristics of sidewall polymer after metal RIE.

The etched profile in metal RIE is achieved by controlling the polymer deposition on sidewalls. The sidewall polymer is key in preventing isotropic etching of the Al(Cu) by Cl radicals. However, it must remain thin enough to not introduce taper in the sidewall profile. The addition of  $\text{N}_2$  to the etching gases can affect the integrity



**Figure 41**

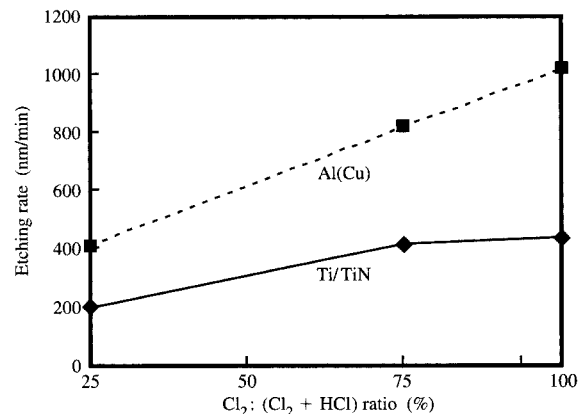
SEM of a void ("mouse bite") caused by corrosion on an Al(Cu)-based wire.



**Figure 42**

SEMs illustrating the effects of  $N_2$  on wire profile. Top: Insufficient  $N_2$  was added, leading to undercutting of the Al(Cu) below an upper layer of TiN. Bottom: A sufficient amount of  $N_2$  was added, preventing the undercutting.

and the thickness of the polymer. An excess of  $N_2$  can lead to a relatively thick buildup and tapered sidewall,



**Figure 43**

Etching rates vs. reactant gas-flow ratio. Similar effects can be observed using a  $Cl_2/BCl_3$  mixture.

while too little  $N_2$  does not provide sufficient buildup.

**Figure 42** contains SEM micrographs showing the effect of adding small amounts of nitrogen to control the sidewall profile. The addition of nitrogen alone does not control the profile. An additional influence on the profile and sidewall passivation is the quantity of resist-etching by-products in the plasma. By controlling the loss of resist, the metal profile can be changed. This is done by selecting suitable RIE process conditions that generate the best anisotropic etching conditions. A balanced process must be found to control the top loss and subsequent redeposition of the resist mask. It has been found that significant process control can be achieved when an ICP is utilized for metal etching.

#### Other metal RIE requirements

In addition to the emphasis on corrosion prevention, other challenges in the etching of Al(Cu)-based wires are listed in Table 6. One of the key parameters is the Al(Cu) etching rate. Higher etching rates are needed in order to minimize process time. Higher rates are also needed to offset the additional time required for post-metal RIE treatments (resist stripping, rinsing, etc.). The etching rates of the Al(Cu) and the Ti/TiN layers are dominated by the gas-flow ratio, as shown in **Figure 43**. However, the optimization of the gas-flow ratio, as well as other system parameters (e.g., rf bias power and pressure) is important for achieving etching-rate uniformity, control of sidewall buildup, and minimization of residues. The effects of other process parameters such as rf power on etching-rate uniformity have been discussed in detail elsewhere [67].



Aspect-ratio-dependent RIE behavior associated with microloading effects becomes more significant for sub-0.25- $\mu\text{m}$  etching. The data reported by Yang et al. [68] indicate that the etching rate decreases considerably for high aspect ratios and that there is a linear decrease in etching rate with increasing aspect ratio. The data show the drop in etching rate for different conditions of pressure and gas-flow rates in an ICP reactor at different plasma source and wafer bias power settings, and indicate that the drop in etching rate for high aspect ratios is less pronounced when  $\text{BCl}_3$  is replaced with  $\text{HCl}$ .

The presence of metal residues remaining between metal lines on chip wires can lead to electrical shorting. There are several mechanisms that lead to such residues. The most widely accepted is attributed to Cu precipitates [69]. Small amounts of Cu are added to the Al wires to improve their resistance to electromigration-induced failure. The amount of Cu added to Al is usually 0.5%. Even with this small amount of Cu in the alloy, precipitation of Cu occurs, and Cu etching by-products in the form of copper chloride are formed. Copper chlorides are involatile at low temperatures and can leave a residue on the wafer surface. Sato and Arita [70] have reported that the high temperatures necessary to volatilize copper chlorides ( $>200^\circ\text{C}$  [70]) are not practical when resist is present on the wafer. Another type of residue occurs as a result of micromasking. Because of the stress mismatch between the Al(Cu) and the top barrier layer, usually TiN, micropores at the grain boundary triple point are generated. The photoresist developer, usually tetramethyl ammonium hydroxide (TMAH), attacks the metal under the barrier through these pores. The metal is corroded locally by the photoresist developer and etches more slowly than the surrounding metal. The corroded region micromasks the metal lines, forming a conelike residue. According to [70], the source of such "spikes" is the  $q$ -phase Cu. One approach to removing this defect is to control the metal deposition process in such a way that the Cu precipitation can be avoided. This can be achieved by carefully optimizing wafer temperature during metallization. In the literature a variety of techniques are suggested to eliminate the spikes. Typically these techniques require "sputtering off" these residues with inert gases. The problem with such solutions is that they can cause the sidewall profile to become tapered. The micromasking can also occur as a result of Al(Cu) grain collapse related to stress mismatch between the Al(Cu) and TiN barrier.

### Concluding remarks

Plasma-etching processes used in the fabrication of ULSI semiconductor circuits have been discussed, with emphasis on work in our facility. The extension to 248-nm-wavelength lithography, increased aspect ratio of IC

structures, and novel device layouts requiring high-selectivity etching have required the development of improved etching processes. Hard masks are being used at many levels to extend lithography as resist thicknesses decrease and resist sensitivity to etching processes increases. The use of antireflective coatings is becoming an integral part of the etching process. More stringent linewidth specifications at critical levels, such as the gate-conductor level, and topography induced by other process-integration features require further improvements in etching processes. Accordingly, plasma-etching systems have evolved from the capacitively coupled plasma systems handling many types of films to highly specific, high-etching-rate, inductively coupled and magnetically enhanced systems. The move to reactors in which plasma generation is decoupled from bias power (e.g., HDP sources) is becoming more popular because of the additional flexibility such reactors provide. Because of their higher cost, their use will be limited to only those applications where they are needed; low-cost conventional alternatives will continue to be employed in less critical applications. This mix of reactors should be sufficient to meet the plasma-etching needs of the next several generations of logic and DRAM chips. As processing evolves from 200-mm to 300-mm wafers, continued improvement is required in process uniformity, requiring improvements in gas-flow dynamics and wafer-temperature uniformity. New gas mixtures must be developed to provide the improved selectivity necessary for novel integration schemes. By interacting closely with the lithography, process integration, and design disciplines, the plasma-etching discipline should successfully provide solutions for a variety of future IC processes.

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